Warsaw ELHEP Group

Research Visit Summary

at DESY, TESLA-XFEL

31 January - 22 February 2004

Institute of Electronic Systems
Warsaw University of Technology

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Warsaw ELHEP Group for TESLA (XFEL), 31.01-22.02, 2004

CONTENTS

/document compiled by dr hab.R.S.Romaniuk/

Summary

1. FPGA based SCCav SIMCON (ver.1.0), containing a single channel cavity simulator and controller, was made fully operable in the industrial conditions; The processing potential of this device of new generation is around ten times bigger than any other technology used so far for the LLRF system. Optimization process may increase this potential even more.

2. Full, three layer, documentation is under preparation for the SCCav SIMCON ver.1.0, enabling cavity model, hardware and software reproduction;

3. The design of the ver 2.0 of SIMCON is advancing; BMB and DBs are under tests and debugging; Improved version of BMB is being prepared for production;

4. Design of ver 2.1. of SIMCON is preliminarily considered; New assumptions are considered for much bigger role for fast photonic data transmission and concentration of data from converter board via an FPGA chip;

5. Design of ver.1.0. of RF Gun SIMCON has just started; From the hardware point of view it is identical with SCCav SIMCON ver.2.0; The only difference is in software; Thus, only the latter nomenclature would be maintained – SIMCON ver.2.0 and 2.1. ;

6. A number of very important conclusions were drawn from the development and application process of the SIMCON, ver.1.0. One of the most important is that the next generation of the LLRF should definitely base on FPGA, mixdes (wherever possible) and multigigabit photonics.

7. Plans are under discussion, relevant to further research involvement of the ELHEP Group in the XFEL accelerator; The Group understands its role only as a research team on new generation of the LLRF systems;

8. New publications are under preparations for the peer reviewed journals NIM and IEEE Trans. Nuclear Sciences; The discussion is now carried within the Group and externally on the relevance of parallel publications in the TESLA Web and the archival journals.

9. The major conclusion is that the Group, basing on the experiences with the SIMCON ver.1.0 and technologies applied therein, may undertake the effort of building a full scale industrial model of the digital part of the LLRF system for the SC accelerator of next generation. The design should definitely base on the FPGA-photonic solution. This is a technology of choice, now the major industrial trend. Resignation from using of this trend means a lot more required effort for own solution design, thus, more time and money for the project.

1. Introduction – Group statement and status of technology

This design bases on two major assumptions: the need for much bigger processing power of the electronics for the accelerator LLRF system and the need for much bigger data concentration and transmission rates. The first is available through the application of the newest solutions of the FPGA chips with enhanced logics, DSP, memory blocks, embedded PC and multiGbps optical interfaces. The second is available through multigigabit fiber optic systems cooperating from one side with massive analog data conversion and concentration and from the other side with very efficient FPGA chips. We do not see any other alternative to these prevailing trends. We would like to use these strong industrial trends efficiently in designing the future LLRF system.

A major breakthrough was achieved during this visit of the ELHEP Group in DESY. The FPGA based version of the simulator and controller for the TESLA XFEL superconducting cavity (SCCav SIMCON, ver.1.0) was made fully operable in the TESLA hall 28. The SIMCON works now with the DSP version of the cavity controller in the full closed loop, including the analog channel. The SIMCON has a great development potential, surpassing all technologies used so far by at least one order of magnitude in nearly all parameters, including speed, rate and bandwidth. For example, the current implementation (without any dedicated optimization) can work 5 times faster than the system of previous generation. The SIMCON is a self sufficient device as it may work with its own FPGA based controller. The implementation of the fully operable combo of the SC cavity controller and simulator in a single FPGA chip (of medium size) shows clearly the maturity of this technology and indicates totally new directions for the future design of the accelerator LLRF systems.

The experiences with the SCCav SIMCON, gained during the design, development, implementation, testing and application processes, allow us to undertake the next task to build an analogous FPGA based SIMCON system for the RF Gun “hot” cavity. The modifications of the FPGA system for other accelerator cavities functioning in DESY and elsewhere would be possible. Using the recently recognized and mastered methods, the design process might be much faster, less effort consuming and much cheaper.

The new generation of the LLRF system, with its tremendous capacity, would enable adding a number of new functionalities. The new generation of the accelerator LLRF system should base, in the widest extent, on the FPGA-DSP processing and fast multigigabit optical transmission The new functionalities, available in such a new generation of the system, may include:

- greater value of the intermediate frequency, (from 250kHz to 2,5MHz);
- considerably bigger trigger rate of the system, (from 5Hz trigger to 50Hz and more, like 500Hz); the confinement is a klystron, not electronics;
- more measurement channels per cavity, (from 1,2, to 6 and more);
- inclusion of massive exception handling in the system, (application of trigger architecture);
- running of full factory with real life cavities and simulators and comparing the results of calculations and measurements in the real-time, (full individualization of cavities);

- inclusion of more precise models of the cavity, (nonlinear filling characteristic, especially near the starting point of the flat-top, more precise mechanical model basing on the results of measurements, etc.);
- much more calculations and data processing possible between the system trigger signals;
- individual cavity parameters identification, (precise recognition of cavity parameters and characteristics); multi-cavity simulator;
- FPGA based linearization of ADCs, (increasing the linearity range of the converters);
- mixdes approach, wherever appropriate, (combining analog and digital parts of the system to boost performance and lower costs);
- serving more cavities by a single chip, (efficient usage of immense processing power of contemporary FPGA-DSP chips);
- direct cooperation of the FPGA chip with fast optical channels, etc. (now 2,5Gbps, soon 10Gbps, possibly 40Gbps, and more with the introduction of new standard of 80Gbps); Efficient usage of FPGA chip resources is possible only by concentration of data to be processed via multigigabit channel;

In the light of these practical experiences *(described here and in previous reports of the Group)* ***with the SIMCON ver.1.0, any freezing of the situation with old technologies basing on the classical, power hungry and geometrically redundant VME crates, classical microwave cables, analog electronics, etc., would be probably a great mistake for the future version of the XFEL's LLRF system.***

The ELHEP Group defines its role, with the kind consent of the DESY management and the SC accelerator LLRF system management, as an aggressive research team of the newest available technologies in the FPGA and photonics, for fast mass data processing. Practically speaking, the role is to prove the applicability of the new emerging programmable digital and photonic multigigabit technologies in the systems of concern. The role is to research and next to build useful working models of the needed sub-systems and check them in the real life industrial conditions.

This is the only role, in which the Warsaw ELHEP Group can survive, for longer term, in the demanding research environment in DESY. The ELHEP Group consists of academics and students, thus the style of work is not, and can not possibly be made, precisely industry like. More people and more time is needed for our procedures, than it would be required for business professionals. One of the important conditions to follow the fast pace of project developments by the Group is building the Warsaw mirror laboratory. The big hope for this are sources offered recently by the CARE program.

The gained experiences with the FPGA based SCCav SIMCON, ver.1.0 gives us a solid right to suggest building a full model of the LLRF system basing totally on new solutions in signal processing, data acquisition and transmission. To fulfill this program the Group needs constant access to own, fully functional system copy with real life signals (separate big VME rack). Following the precisely designed stages, the major parts of the LLRF system may be exchanged for the new versions.

The following general schedule is suggested of further work of the Group:
- finishing the ver.2.0. of the backbone mother board BMB and DBs and gathering experience with a design of this size and complexity; production of the second

modified mother board, finishing the TLK version of Opto-board; system application and tests; time: half a year;

- in parallel starting the design of the BMB ver 2.1. Redesign of board and function assignment; design of a new converter board including FPGA with multigigabit SerialLight standard; enhancing the mixdes design of the converter board with FPGA linearizer and controller; enhancing the design of the downconverter board with much higher intermediate frequency; experimenting with O/E converters and serializers working at a rate over 10Gbps, using FPGA with powerful DSP capabilities and direct optical inputs, checking the possibility to enter the optical PCB (PCBs with embedded optical paths) technology, time: a year;

2. Status of SIMCON for SC cavity

This device would be referred further to as SCCav SIMCON. This chapter contains the description of advances in the main task of the team. SIMCON stands for the FPGA based simulator and controller for the TESLA superconducting (SC) cavity. There was a major breakthrough of installing the simulator together with the control hardware of the XFEL linac.
The SCCav SIMCON is a ready and closed product which could be easily reproduced basing on the full set of technical documentation available form the Group and soon made accessible via the TESLA web, as well as in the printed version.
The further part of the chapter contains:

- short technical documentation of the SC cavity SIMCON now in exploitation (ver.1.0). Full version of the technical documentation to be provided separately in a self-contained document;
- status and development plans for the SIMCON for SC cavity, ver.2.0.

The integrated and parameterized control and simulator system (SIMCON) for the SC resonant cavity of the FEL uses a programmable FPGA VirtexII V3000 chip. The chip has inbuilt hardware DSP components [7].

The hardware layer of the system bases on *XtremeDSP Development Kit* by Nallatech [8]. The used version of MPCB in *BenONE* integrated with a DB *BenADDA*. This set of boards, presented in fig. 2, was optimized for realization of fast, hardware based, DSP algorithms. The DB contains two pairs of fast 14-bit A/D and D/A converters and a programmable FPGA Xilinx VirtexII V3000-4 chip. The FPGA chip is equipped in 18x18bit multiplying circuits.

Adaptation of the *XtremeDSP Development Kit* for the usage in the EURO 6HE standard was realized by embedding it in a dedicated base board *6HE-EURO-EPP*. The VME setup was presented in fig. 1. The front side of the board has the following I/O ports:

- two analog inputs of signals in the range of ±1V. Each signal is processed independently by 14-bit ADC, clocked at 40MHz;
- input of external clock signal in TTL standard;
- two analog outputs of signals in the range of ±1V. Each channel signal is processed independently by a 14-bit DAC clocked at 40MHz.
- three digital inputs and three digital outputs in TTL

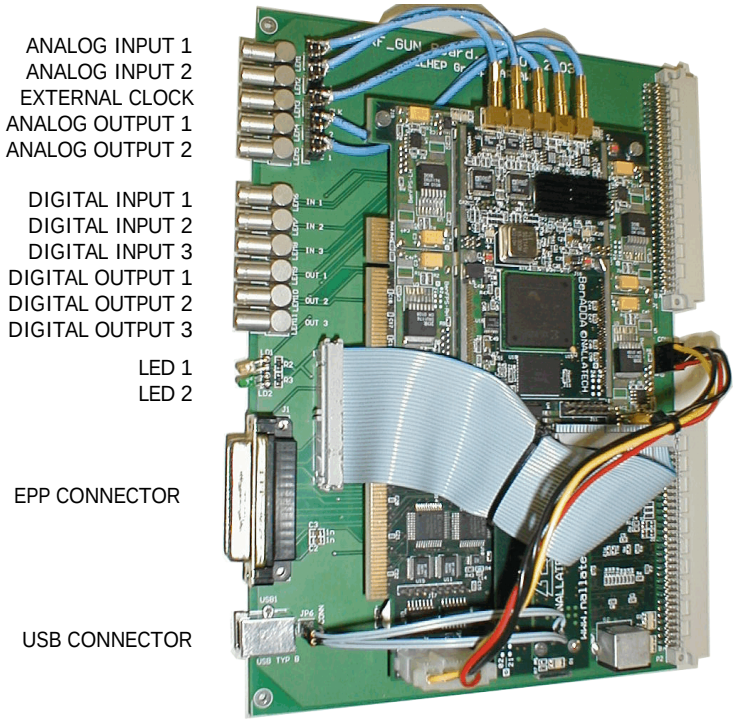


Fig. 1. XtremeDSP Development Kit embedded in EURO-6HE base board.

standard connected via a buffer to the Virtex II chip;

- two information LEDs;
- parallel interface socket in EPP standard. It enables communication of the FPGA Virtex II chip with the controll PC;
- USB interface socket for configuration of the FPGA chip;

The composite SIMCON board occupies two slots in the VME 6U crate. Power supply for the board is provided either via the VME bus or from a proprietary device.

Application of the EPP protocol to communicate with a PC stems from a low throughput of the proprietary USB interface provided by the development board manufacturer. EPP interface was chosen because of wide availability in PC, simplicity of implementation in the FPGA and quite high transmission [2,9].

The integrated SIMCON system was realized from a parameterized structure of functional blocks. The structure was described in VHDL (Very_High_Speed_Integrated_ Circuit_Hardware_Description_Language). The code was implemented in Xilinx VirexII V3000-4 residing on *XtremeDSP Development Kit* board. The AD and DA converters, residing on the *BenADDA* DB, were used for optional connection of signals from external SC TESLA (FEL) cavity simulator or controller. A few digital TTL inputs were installed on the *6HE-EURO-EPP* base board. These were used for synchronization with 1MHz clock and 5 Hz trigger. Both frequencies are distributed via optical fibers by the FEL control system timing network.

The general functional structure of the single channel SIMCON system for the SC cavity (version 1.0) was presented in fig. 2. The applied solution bases on a backbone of parameterized and programmable, parallel processing blocks.

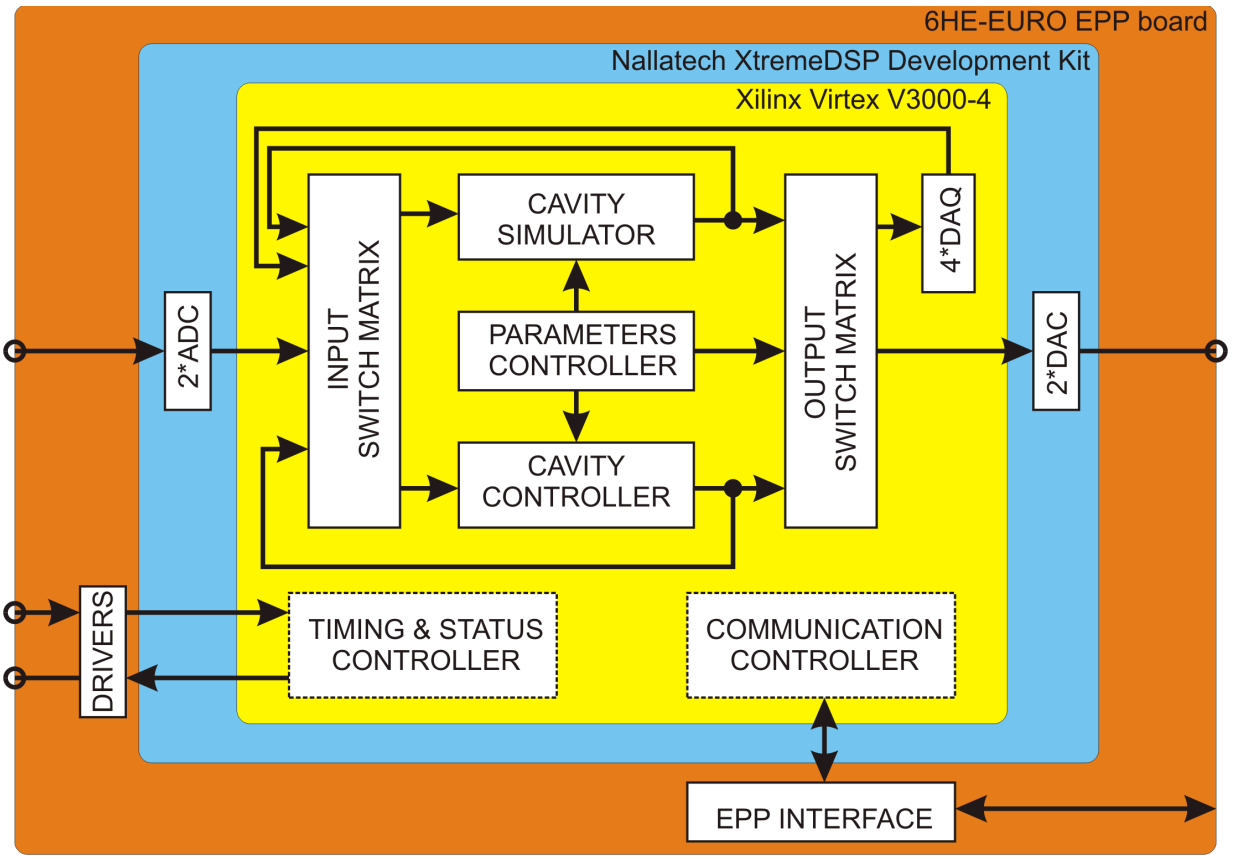


Fig. 2. Multilayer, functional and hardware structure of SC cavity SIMCON.

The core of the SIMCON consists of two independent modules: CAVITY SIMULATOR and CAVITY CONTROLLER. They were programmed in FPGA Virtex II 3000-4 chip as hardware DSP algorithms basing on fast multiplication components. These blocks work in parallel in the real time. They are controlled by programmable parameters provided by the PARAMETERS CONTRLLER block. The parameters are constant values (like I/O amplification of cavity controller, coefficients in the mechanical model of the cavity) and vectors (feed-forward of cavity controller, beam in cavity simulator). The above mentioned pre-set parameters stem from the algorithms, which were described in details in [4,5,6].

The block of INPUT SWITCH MATRIX enables a programmable choice of the control signals for the blocks of the controller and the simulator. Thus, the system may work in several configurations, with connected internal digital feedback or external analog signals from ADCs, or fed with test vectors – pre-programmed in the DAQ block. The task for the OUTPUT SWITCH MATRIX block is a programmable choice of the output signals input for the DA converters or registration of the signals in the DAQ block. A proper configuration of the switching matrix enables appropriate analog feed-back between the modules of savity controller and simulator.

The block of TIMING & STATUS CONTROLLER provides the internal synchronization of all processes inside the whole of the SIMCON system. The SIMCON may work with the external clock of the FEL or autonomously with the internal one. The block enables switching of the work states. The processes may be realized in the real-time as well as be realized in the simulation state with the use of the input reference vectors.

The programming layer of all blocks for the SIMCON, performed via the monitoring computer system, is done by the COMMUNICATION CONTROLLER block. The hardware EPP data transmission protocol is used.

The SCCav SIMCON now in exploitation (version 1.0) bases on the proprietary Virtex development board by Nallatech. This solution was decided for the following reasons: first time undertaken effort to build FPGA based cavity simulator, delivery time and chip availability. This version may be potentially developed further to ver.1.1. with some additional functionalities like readout channels, VME control, etc. However, the development capacity of this version is confined by the number of available analog channels. Now, due to these confinements, the Group decided to enter into the design of the ver.2.0. This version will base solely on the PCB designed by the Group.

SIMCON ver. 2.0. STATUS

The status of the SCCav SIMCON ver.2.0. is as follows:

PCS was designed and fully presented in the previous ELHEP Report;

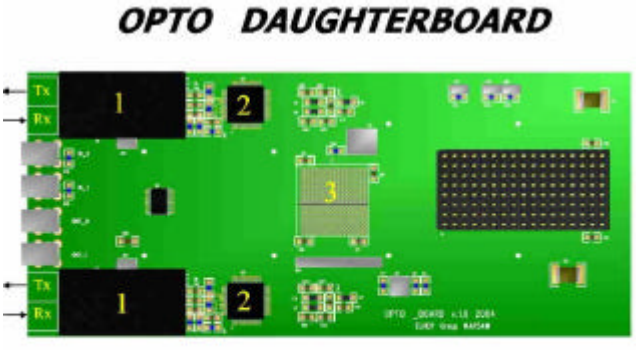
Mother Board and some of Daughter Boards went into production;

there was a mistake in the ETRAX board and the board should be repeated in production,

ETRAX DB now is in production again;

VME DB is ready and debugged;

OPTO board using the TLK distribution is under debugging; see photo beside.



1 - Agilent HFBR5921L 850nm Optical Transceivers
2 - TLK2501 Ser/Des 1.5 to 2.5 GBPS Transceivers
3 - FPGA Altera Cyclone EP1C20F324

The conclusions with initial experiments with the OPTO board and with the ADC/DAC converters prompt for change of the design of this part of the system. The converters and the opto should be combined to a large single PCB. The 2,5Gbps opto-link, may manage up to 16 pieces of 14-bit converters, assuming the upgrade of the intermediate frequency to 2,5MHz. Assuming more signals from a single cavity (increasing from one to two, up to six, including field measurements, forward power, reflected power, etc.) it is wise to think of entering into easily available higher rate optical technologies like 10Gbps. 10Gbps opto-board can manage as many as 64 cavities in the upgraded system.

The processing capacity of the FPGA chip, scheduled for usage in the SCCav SIMCON ver.2.0. Virtex 4000, is so big (but necessary) that the bottleneck of the system is to provide efficiently the data for this processing. To avoid this bottleneck, a lot more effort should be placed to the design of DAC/ADC board and very fast OPTO link board.

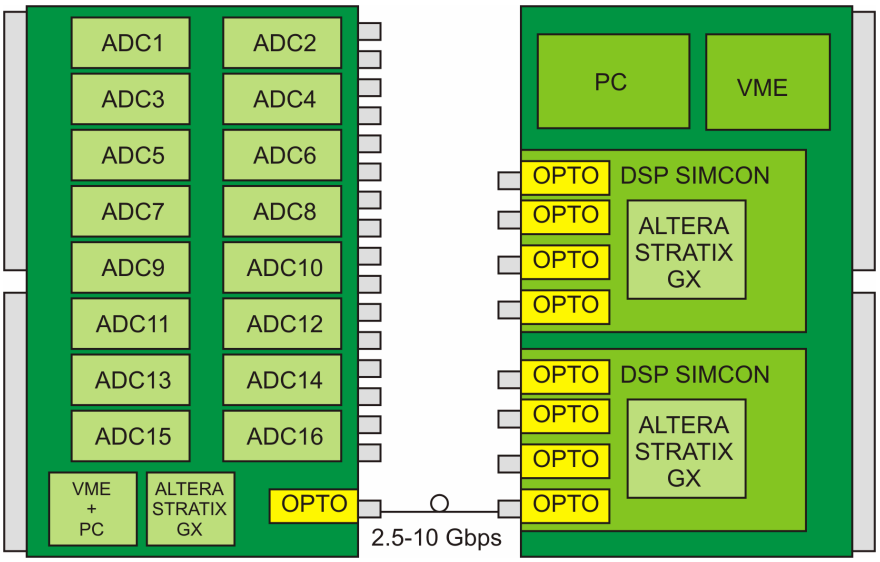


Fig. Data concentration idea based on multichannel ADC board, FPGA concentrator and fast fiber optic data transmission. The system structure embraces:

1) analog concentrator with optical transmitter;
   Proposed version: 16 analog channels, 2.5Gbps, Altera StratixGX 25
2) DSP concentrator with optical receivers;
   Proposed version: 4 optical receivers 2.5Gbps (later 4x10Gbps), Altera StratixGX or/and Altera StratixII

The proposed measures are:

Place the converters as close to the analog signal measuring site as possible and integrate with this board a very fast optical transmission channel.

Design the converters board flexibly to enable the exchange of the converter chips (placed on exchangeable insert);

Use serial-light standard introduced by Altera and implemented in GX series of Stratix FPGA chips, direct connection of optics with the DSP.

Design version of 2.2. opto-board basing on Stratix GX 25 chip; buy a few chips of this kind;

Start to experiment with the GX series of FPGA chips;

The human resources working for the design of this part of the system have to be essentially increased; I suggest increasing it by two people; The candidates are M.Sc students Mr Jerzy Zielinski and Krzysztof Olowski;

Increase the hardware base of the ELHEP barrack number 28F located near the east wall of the TESLA tunnel close to the RF Gun by:

- localization of a next big VME rack in the barrack with full system functionality, spanning from signals from real cavities, downconverters, ADC converters, cavity SIMCON, DAC converters, all system timing and control; If it is not possible, reserve a place for such a big rack adjacent to the east wall of the tunnel.
- provide one big rack to be taken to ELHEP laboratory in Warsaw; the racks are readily available from the DESY Lager;

The preliminary schedule for this task is as follows:
1. The SCCav SIMCON board, ver. 2.0. is under last stages of the design now,
Parts of the board entered into production a few months ago, the remaining parts should go to production as soon as possible, The board will contain full six channel DAC/ADC, two pairs of I/O,
2. Algorithm should be enriched to include further functionalities;
3. Hardware debugging is continued and should be finished in May
4. Board should be ready by the end of September
5. In parallel, the design process goes on over the version 2.1. with reworked and extended part of converters and opto board. The specifications of the experimental boards collection is under preparation. DSP and opto part of this board design will be ready soon and will be ready for production in March.

A new proposal is that the Group may enhance the activities around the new version of the RF downconverter. We may consider, upon the consent of the LLRF group management, adding one more person to help Mr Guenther Moeller with the work on the device. We are considering to make some trials with intermediate frequency of 2,5MHz instead of 250kHz.
The possible candidate is Mr Tomasz Filipek, M.Sc student working on fast analog systems.
One of the possible design options would be so called mixdes (mixed design including analog and digital parts) version of the downconverter and ADC board. The boards may contain FPGA matrix, serving for example to linearise the characteristics of the ADC.

References

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2. K.T.Pozniak, R.Romaniuk, K.Kierzkowski: “Parameterized Control Layer of FPGA Based Cavity Controller and Simulator for TESLA Test Facility”, TESLA Technical Note, 2003-30
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7. http://www.xilinx.com/ [Xilinx Homepage]
8. http:// www.nallatech.com/ [Nallatech Homepage]
9. http:// http://www.beyondlogic.org/epp/ [EPP - Enhanced Parallel Port description]

3. RF Gun Controller and Simulator

A new task defined during 2003 WILGA Symposium. The requirements were gathered during this time and an outline for the RF gun algorithm was prepared. Now the RF gun system was defined in a form of a signal flow block diagram. The Group decided to undertake the effort to build a full operable hardware model of the SIMCON for the RF gun. The model will base on the previous experiences with the SIMCON for the SC cavity.

There is the same solution of the hardware with the SCCav hardware. The difference is only in the loaded algorithm in the FPGA chip.

The preliminary schedule for this task is as follows:
1. The RF Gun board is under design now,
The board should go to production as soon as possible, The board will contain full eight analog input channels, four full analog output channels,
2. Algorithm should be ready by the end of April,
3. Hardware debugging should start in May
4. Board should be ready by the end of September

The work on the SIMCON hardware (for SCCav and RF Gun) is integrated with the work on middle-layer functional software and GUI. The GUI is under design and tests in several versions including: DOOCS, Java, Web, SCPI, etc.

4. Radiation sensitivity of components for TESLA XFEL

A program of radiation experiments is under preparations with the participation of several persons from the Group (D.Rybka and A.Kalicki) and dr Bhaskar Mukherjee from the radiation sefety Group of DESY.

The nearest plans include:

- construction of GaAlAs LED based remote on-line dosimetry;
- irradiation of LEDs in Warsaw Heavy Ion Cyclotron;

Other tasks are:

1. Comparizon between responsivities of CCD and CMOS cameras
2. Tests for SEU of FPGA board

5. Warsaw ELHEP Laboratory status - update for TESLA XFEL

The Group has recently consolidated again its activities around several topical lines. These topical lines were updated after finishing the first version of the SCCav SIMCON. The major topical lines are coordinated by more experienced members of the Group (Ph.D. students).

The following topical groups are defined with their leaders:

1. DIAGNOSTICS (diag)
leader: Tomasz Jezynski (Ph.D. student)
subject: Diagnostic system for TESLA (XFEL) including technical data base for TESLA
Will base on the applied solutions for BAC/ZEUS detector.
persons: Piotr Pucyk (70%),
Adam Grodecki,
Jaroslaw Szewinski;

2. DATA QUALITY MANAGEMENT (dqm)
leader: Piotr Rutkowski (Ph.D. student)
subject: data quality management, DOOCS, Web Interface, Java,
persons: Piotr Pucyk (30%),
Waldemar Koprek, data base for TESLA and SCPI interface;
Pawel Kaleta,
Radoslaw Wójtowicz;

3. PCB DESIGN, HARDWARE (pcb)
leader: Wojciech Giergusiewicz (Ph.D. student)
subject: pcb design, Protel, DSP, OPTO, 10GbE,
persons: Jerzy Zielinski,
Krzysztof Olowski,
Karol Perkuszewski,
Wojciech Jalmuzna;

4. MODELING (mod)
leader: Tomasz Czarski (Ph.D. student)
subject: MatLab modeling of SC cavity and RF Gun cavity, Direct hardware control from MatLab;
persons: Tomasz Filipek, quadrature detection, I Q vector modulator and demodulator, output signal for klistron control, frequency downconverter, mixdes technologies, FPGA based linearisation of Adcs;
cooperation of T.Filipek with H.Wedding and G.Moeller;
one new student,

5. RADIATION (rad)
leader: Dominik Rybka (M.Sc. student)
subject: radiation hardness of TESLA XFEL electronics (components and sub-systems)
persons:
cooperation with dr Bhaskar Mukherjee
Arkadiusz Kalicki, software for SSD and CMOS cameras, image processing, LabView,

one new student

6. EMBEDDED TECHNOLOGY and SYSTEM on CHIP (soc)
leader: dr Wojciech Zabolotny
subject: embedded systems, micro PC, micro linux, system on chip (soc),
persons:
Piotr Roszkowski,
Krzysztof Husejko,
One new student,

7. FPGA/VHDL
leader: dr Krzysztof T.Pozniak
subject: FPGA based system design, VHDL description, internal interface middleware, general system outline, system design and coordination,
persons:
ing. Krzysztof Kierzkowski, system design, PCB, hardware, laboratory, measurements, Protel,

8. Warsaw ELHEP Laboratory
leaders: Ryszard S.Romaniuk and Krzysztof T.Pozniak
subject: hardware and software for Warsaw ELHEP mirror laboratory, FPGA based hardware design – multigigabit OPTO, VHDL, FPGA, PC cluster, GRID; software – MatLab design and hardware control, VME;
persons:
Karol Perkuszewski, hardware
Wojciech Jalmuzna, hardware
Radoslaw Wojtowicz, hardware
Pawel Kaleta, software
Bartosz Jablonski, software
Jaroslaw Szewinski, software

9. WILGA
leaders: each two years different student representative; Waldemar Koprek, Krzysztof Olowski and Jerzy Zielinski for 2004;
subject: organization of annual IEEE-SPIE symposium in Wilga on Photonics and Web Engineering for HEP experiments;
persons: 2004 – Waldemar Koprek, Krzysztof Olowski, Jerzy Zielinski, Arek Kalicki, Michal Ostapowicz, Adam Grodecki,

The above micro task groups can be gathered in two macro task groups: hardware and software. The hardware macro-group is managed by dr K.Pozniak and integrates the activities of the micro-groups 3,4,5,6,7,8. The software macro-group is managed by T.Jezynski and integrates the activities of the micro-groups 1 and 2.

6. Persons participating in the current visit

R.S.Romaniuk 31.01-22.02; K.T.Pozniak 31.01-22.02, T.Czarski 31.01-29.02; W.Giergusiewicz 31.01-22.02; P.Rutkowski 15.01-15.02

7. Update of planned visits for the nearest 6 months

Ryszard S.Romaniuk - 17.04-09.05;
Krzysztof T.Pozniak - 17.04-09.05;
Grzegorz Pankanin - 24.04-03.05;
Waldemar Koprek - 17.04-03.05;
Piotr Rutkowski - 08.03-05.04; 15.04-13.05;
Tomasz Czarski - 21.03-04.04; 17.04-16.05;
Piotr Pucyk - 01.03-31.05
Dominik Rybka - 01.03-25.05;
Wojciech Giergusiewicz - 21.03-25.05;
Jerzy Zielinski - not yet defined, engaged in new opto-board design
Krzysztof Olowski - not yet defined, engaged in new opto-board design
Tomasz Jezynski (not at DESY) 6-14.04; 14-27.06; 31.07-4.08; 6-19.09
Tomasz Filipek – not yet defined, possibly April, engaged in downconverter and HF analog electronics;

Tasks of the individual persons are defined in chapter 5.

8. Update of publications plans

The Group has recently published the results of its work in 12 TESLA Reports published on the TESLA web. A question was forwarded to Dr Robert Klanner, editor of the NIM Journal (by Elsevier) what are the possibilities to publish the results in a peer reviewed and archival type of journal.
If there is any contradiction between these two types of publications (actually three: Internal Technical Reports, Conferences and Archival Journals, the Group intends to concentrate, in the future, its publications on the latter).
A few papers are in preparations for NIM and for IEEE Trans on Nuclear Sciences.

9. Update of conference plans

WILGA 2004 Conference on Advanced Electronics and Photonics for HEP Experiments is scheduled for 26-30 May
ELHEP representative will participate in LINAC 2004 (XXII Linear Accelerator Conference) in Lubeck on 16-20.08.2004;
WILGA 2005 Conference will be organized within a large SPIE Congress on Photonics in Warsaw on 28.08-2.09.2005