Warsaw ELHEP Group

Research Visit Summary at DESY, TESLA

06 September - 06 October 2003

(TECHNICAL REPORT)

Electronics for High Energy Physics Experiments; tel. 8998-1955;
http://nms.ise.pw.edu.pl/elhep; email: rrom@ise.pw.edu.pl
Institute of Electronic Systems (ISE), Warsaw University of Technology (WUT)
Institute of Experimental Physics (IFD), Warsaw University (WU)

CONTENTS

Technical Report compiled by Dr hab.Ing. R.S.Romaniuk, ELHEP.

SUMMARY

1. Summary of work done

2. Purpose and tasks
1. General purposes of visit:
1. TESLA Cavity LLRF Controller and Simulator
2. TESLA RF Gun Controller
3. DOOCS interface
4. Radiation hardness of electronics in TESLA Linac

2. General Tasks:
Tesla Cavity Simulator and Controller modeling by modern tools (MatLab, Simulink, etc.)
Tesla Cavity Simulator and Controller Description in VHDL
TESLA RF Gun controller – preliminary considerations
Hardware and software development program
Prepare equipment to be ready for TESLA Linac operation (all persons involved)
Preparations of hardware for first trial to mount equipment at the liniac (all)
Prepare background set-up for radiation investigations of electronics at Linac II
Preparations for hardware implementation in VME crates
Initial tests of radiation hardness of electronics for TTF
Tests of cavity simulator
Integration with cavity controller
Preparing Xilinx development boards for tunnell installations
Set-up of all necessary auxiliary equipment
Further Xilinx development boards and software tests
Start design of VME development board

1. Persons and periods of stay in DESY
Ryszard Romaniuk (06 September-06 October), Krzysztof Pozniak (07 - 22 June), Piotr Roszkowski (15 - 22 June), Tomasz Czarski (26 May –05 July), Piotr Rutkowski (26 May -14 June, 22 June – 27 July), Tomasz Jezynski (permanent stay), Krzysztof Kierzkowski (09 – 14 June), Dominik Rybka (ELHEP student, 14-29 June and 07 July – 31 August) and Piotr Pucyk (ELHEP student, 14-29 June and 07 July – 31 August).

Contributions of individual members of ELHEP Group (summary)
Tomasz Czarski: cavity controller modeling, trials to combine MatLab model with hardware, cavity simulator, step model integration with hardware
Krzysztof Pozniak: VHDL internal interface, hardware set-up and internal interface advancements
Dominik Rybka: radiation tests program for FPGA control boards; preparations for a seminar on radiation tests of Tesla electronics at LINIAC II
Piotr Pucyk: DOOCS study and cooperation with Dominik Rybka
Krzysztof Kierzkowski: hardware set-up, design of prototype test board
Wojciech Zabolotny: MatLab/FPGA model of cavity simulator, cavity controller checks and tests with simulator
Piotr Rutkowski: C++, software for TTF electronics

Tomasz Jezynski: laboratory set-up, hardware tests; diagnostic system for Bac detector – the
system may be adapted in case of need for TTF purposes. The system features channel calibrations, efficiency mapping, configuration, graphical visualization.
Zbigniew Luszczak: LLRF database, GUI interface, Database software BacNavigator+BacViewer, now available on zwalab5.desy.de may be adapted in the future for TTF purposes. This software is modular and reconfigurable and allows to view all detector resources
Ryszard Romaniuk: Electronics radiation in Linac II, Cavity controller modeling, hardware set-up, own test board design, team effort coordination, publications preparation, team report coordination and edition, M.Sc. and Ph.D. students supervision, ELHEP TESLA Reports edition;

1. ELECTRONICS FOR LLRF TESLA – two layer approach

This document describes, in a general way, the basic properties of the FPGA based electronics boards needed for the LLRF simulation control and diagnostic system for the TESLA. The boards design was done by ELHEP. It is suggested that the electronic system for the LLRF has two layers:

- constant hardware environment (CHE) capable to accommodate all processing needs of the LLRF with proper redundancy, and to some extend nondependent from these needs,
- LLRF task oriented electronics (LLRFE), realized as small, cheap and exchangeable blocks, submerged in the constant hardware environments and using the necessary resources of the CHE.

The CHE will be realized in a form of the backbone mother board (BMB) supplemented with a few technical daughterboards (DB). These DBs will be responsible for the I/O and fast communications with the outer world (preferably computer network) and with other BMBs.

The LLRFE will be realized as task oriented DBs residing on the BMB. The boards will realize such tasks as: RF gun controller, Cavity controller and simulator (cavity factory), cavity microphonics piezocontroller, exception handling, other tasks to be defined, etc.

The major idea behind this two layer approach is to insulate the LLRF tasks from the hardware backbone. The flexible FPBA based backbone may be ready to receive and realize a range of LLRF tasks in a more modular way.

1. 1. BACKBONE MOTHER BOARD (BMB)

1.1. Introduction

The Backbone Mother Board (BMB) is a hardware operational platform for the realization of the functionalities required by the LLRF TESLA sub-systems. These sub-systems include: cavity controller, cavity simulator, RF gun controller, microphonics piezocontrol, exception handling, etc.

The BMB assures standardized communication system basing on the embedded processor and the optional VME interface module.

The main construction idea relies on gathering of all necessary functionalities on a single PCB called a backbone MB. Such a solution allows for modification, choosing and modernization of functionalities without the immediate need to change all of the hardware operation environment.

The major functional aim of the BMB is to gather all of the constant or standard system tasks as: supply, communications, loading the FPGA, etc.

1.2. Board description

The BMB was designed as 6HE-EURO standard. Uses a single value 5V power supply from a standard VME bus. Eight layer PCB is applied. The width of the BMB is double slots. BMB contains up to six-seven daughter boards (DB) placed on its both sides.

1.2.1. Daughter Boards for BMB

The BMB possesses the following DBs: PC processor board (PCB), VME interface board (VMEB), fast synchronous communications board (COMB or OPTOB) to four or five universal A/C and C/A I/O boards (LLRFB). The individual LLRFB are expected to have 8 analog inputs each, thus, four LLRFB warking on a single BMB may have 32 ADC inputs.

1.2.2. Main BMB FPGA control chip characteristics

The tasks of the main FPGA chip residing on the BMB are: provide communications between the PC and VME slots and the rest of the slots available on the BMB; distribution of control signals; loading of the FPGAs residing on the DBs. The chip is loaded directly from the processor or through the VME.

1.2.3. Software for BMB

The software for the BMB was written in VHDL.

1.3. Costs and fabrication time of BMB

Estimated fabrication costs are 800 Euro for a single BMB board with documentation.
Estimated fabrication costs are 1600 Euro for three board with documentation and shipping.
Fabrication time of the board at ITR Warsaw is six weeks.
Estimated costs of the parts for three BMB is 300 Euro.
Aggregated costs for three BMB is approximately 1900 Euro.

1.2. BMB DOCUMENTATION

Included as an appendix

2. DAUGHTER BOARDS FOR BMB

2.1. PC BOARD (PCB)

The PCB is a central board for the computer control of the whole system. The PCB assures standardized communications with the BMB through a facility called the Internal Interface (II). The II is realized in the FPGA. The communications with the external computer systems is done through the Ethernet.

2.1.1. Etrax Board

Now the PCB design uses ETRAX chip (previously it was ELAN chip). The ETRAX chip data are: f=100MHz, RAM=16-32MB, FlashMem=2MB, Eth=10Mb/s. The flash memory contains a boot manager. The Etrax board runs on the embedded ET linux OS. The software initialization of the ETRAX PC is done through the Ethernet.

2.1.2. PCB Software

PRo did essential software for connection of a single chip micro PC to the backbone MB (BMB). The software communicates the PC chip with the FPGA chips over the system.

2.1.3. FPGA Internal Interface Controller (IIC)

II Controller uses FLEX EP10K100RG240 chip. The IIC performs conversion/translation of the local port, implemented it the PC chip (now ETRAX), to the II standard. The IIC chip communicates directly with the PC chip. The II standard is: 32 bits of data, 32 bits of

address, 5 lines of control and 8 lines of interrupts. The code is written in VHDL. The initialization and loading of the IIC is done directly from the PC chip.

2.1.4. Costs and fabrication time of the PC board

The estimated costs of three PCBs at the ITR is 500 Euro.
The estimated costs of components for three PCBs is 400 Euro.
Aggregared costs of three PCBs is 900 Euro.

2.2. VME INTERFACE BOARD (VMEB)

VMEB is a small board supplementing the BMB with VME communications. Together with the PCB it will occupy a single slot on the BMB.

2.2.1. Main VMEB chip characteristics

The VMEB bases on FPGA Altera EEPROM EPM3128A. It works as a converter of the VME standard onto the II standard. Additionally the VMEB is equipped in drivers converting 5V of VME power supply to the 3,3 V of the II. Th voltage of 3,3 V is required for all new FPGA chips. Working with VME is over 32 bits of data, 24 bits of address in the slave regime. The software for the FPGA of VMEB is written in VHDL.

2.2.2. Costs and fabrication of VMEB

The costs of three VMEB is 600 Euro. 500 Euro for the printed circuits boards and 100 Euro for the components.

2.3. FAST SYNCHRONOUS COMMUNICATIONS BOARD (COMB)

The main aim of the Communication Board (COMB) is reception of control and clocking signals from the accelerator LLRF system and fast synchronous data transfer between a group of the BMBs or DBs. There are applied chips of SERDES type, for example: TLK2501, and transceivers – multigigabit Agilent. The board contains the redistribution sub-system for optical signals.

2.3.1. Main chip characteristics of COMB

The COMB is managed by an FPGA chip. The chip realizes control of the transmission and data processing functionalities of the board.

2.3.2. Costs and fabrication time of COMB

The costs of three COMBs is 900 Euro. 500 Euro for the boards and 400 Euro for the electronic parts including FPGA and optical gigabit transceiver. Fabrication time at ITR is 6 weeks.

2.4. LLRF BOARDS (LLRFB)

These boards realized as standardized DBs are responsible for measurements and control within the LLRF system. The LLRFB have to possess appropriate number of analog I/O channels together with a number of ADC and DAC and amplifiers. The following parameters have to be defined: number of channels per a single DB (preferably 8),resolution of the converters (between 14 and 16 bits), frequency of sampling (between 40 and 60 MHz), signal levels, signal quality, noise level, etc.

2.4.1. Main chip characteristics for LLRFB

The FPGA, of relevant resources, realizes processing algorithms for the functionalities required by the LLRF and its particular objects like a cavity, gun, etc. The LLRFB has to

include DSP blocks, internal memory blocks and appropriate logical resources. The requirements of the algorithms are demanding. The applied chips have to be of Xilinx Virtex II or Altera Stratix type.

2.4.2. Costs and fabrication time of LLRFB at ITR

Cost of realization of three LLRFB is approximately 1000 Euro in multilayer (expected 10 layers) printed board technology. Fabrication time may be around 6 weeks.
The major cost is in the components, namely the main FPGA chip for measurement and signal processing for a particular LLFR task.
Now the costs of Virtex and Stratix chips having around 5MG starts from 2kEuro per piece.

3. AUXILIARY BOARDS

3.1. EPP-VME CONTROLLER

(FPGA VME-PCB and software driver)
The EPP-VME controller, basing on the Altera FPGA, was made operable. This PCB has been recently done by the ITR in the VME format. The board was populated and (hardware) debugged (by KK and KP). Software drivers for PC (and later possibly for a Unix
workstation) are under construction (by TJ and PP). The EPP-VME controller was tested with a different VME board (called a pulser) to check the VME read/write access. Standard rate of communication, via a PC LPT connector reaches 60 kilo-operations per secon (kops), for 8 checking bits, 24 address bits and 32 data bits. It is quite a result, since the LPT port has only 8 data bits. We transmit now 8X8 bits (checking, address and data).
The further development potential, not exploited yet, is to use
DMA transmission at a full rate of nearly 120kops (only data, no address).

The versatile, FPGA based, EPP-VME controller board may be very useful for many simple VME applications. The full VME controller is rarely needed in a number of smaller aplications. The estimated cost of this board when manufactured in a short series (more than 10 pieces) will be below 500 Euro. Comparing that with
2kEuro of the full VME controller, gives you perhaps a competitive price of a very useful product. We may offer this product for other TESLA applications. A similar situation may be with the versatile backbone mother board and especially with the micro PC board (initially ETRAX by AXIS, later perhaps Crusoe by Transmeta).

Don't you think that it would be wise, perhaps, to have a few copies of such a simple and cheap but useful EPP-VME controller board to be able to offer other groups in Tesla and DESY.

4. FPGA RF GUN CONTROLLER

We finished all essential work on the EPGA RF Gun controller. Soon we will send you some detailed results. The RF Gun controller works with the real signals with the open loop. Mr H.Weddig strongly adviced us not to mount it now in the crates close to the

tunnell and laser container. The board for the RF Gun controller needs mechanical and layout reworking and may be ready for November tests, if we start the reworking now.

Task definition:
Tasks for FPGA based RF gun controller were defined preliminarily.
The experiences with LLRF control system for Tesla cavity will be adapted and reworked for Gun purposes.

Results and deliverables:
Preliminary control algorithm was suggested.
Works started on gun modeling in MatLab

Near term plans :
Repeat and adapt efficiently the design pathway of cavity controller for the RF gun

5. FPGA CAVITY CONTROLLER

Task definition:
Preparing of laboratory set-up for tests of cavity controller and cavity simulator,
set up enables control,
setting parameters of cavity controller
testing of cavity controller with analog cavity simulator
integration of Mat-Lab with hardware cavity controller at step-like work mode;

Results and deliverables:
Two Tesla Notes published 2003-20 and 2003-21 concerning development in cavity ontroller modeling and FPGA model implementation
FPGA based cavity controller was excited with Chechia input signal and gave output comparable to that from MatLab model.
MatLab model was excited with real cavity signal too.
Preparations go for on-line work of the FPGA controller and short term reliability tests.

Near term plans :
Implementing of the Xilinx Development Boards in the live LLRFC
Hardware and software development program.

6. FPGA CAVITY SIMULATOR

The work on the FPGA based cavity simulator is being progressed in the direction to use only the pure VHDL technology basing on matrix manipulations and not the SysGen. The simulator was done in the SysGen version but it is not promising technology at all.

Task definition:
Design of digital model under Xilinx core generator was performed.: main parameters - 64bits of accuracy at 40MHz clock
New version of cavity simulator is under development.
The model bases more on VHDL.
Model design is shifted from Xilinx core generator to own VHDL solutions.

The aim is to minimize the size of the design.

Results and deliverables:
One Tesla Note was published 2003-23 concerning DSP realization within FPGA for Cavity simulator.
Parameters of the simulator were calculated.
Simulator was tested with cavity controller in a control loop.

Near term plans:
Apply the simulator in the whole model of the working factory

7. RADIATION RESPONSE OF ELECTRONICS

Radiation response of electronics is performed in the Linac II.

Radiation hardness investigations of LLRF electronics for TTF II

Task definition:
Subject of the effort is using Liniac II as a test bed for gamma radiation (and perhaps neutron) influence on LLRF electronics for TTF II
Additional person from ELHEP to be involved in the program;
Needed hardware, software and experimental set-up to be assessed;
Experimental program details to be established.
Participation in preparation of experiments on radiation hardness of electronics in LINIAC II
Assembling of parts of experimental set-up.
Experiment operators defined.

Results and deliverables:
Video server initially established.
Started gatheruing images from the camera on the first vehicle
The need for second vehicle and its armament defined
Signal connected Xilinx board inserted in the tunnel of Linac II
First measurements just started

Near term plans:
Second vehicle with blind camera
Possibly third vehicle with FPGA board
Systematic data acquisition system has to be implemented

8. DOOCS INTERFACE

DOOCS interface is under construction for the electronics the group is doing. It includes DOOCS clients for the boards and later DOOCS server.

TESLA DOOCS and LLRFC system database
Task definition:
The Distributed Object Oriented Control System http://tesla.desy.de/doocs/

Participation of ELHEP in DOOCS System, Considerations to prepare Doocs server-client for Cavity Controller
Work just started by P.Rutkowski, P.Pucyk, D.Rybka
Meeting with dr Kay Rehlich and dr S.Simrock , R.Romaniuk and Zbigniew Luszczak. Dr S.Simrock prepared LLRF database concept document. Z.Luszczak of ELHEP is considered as a person participating in database preparations and development.

Results and deliverables:
Defined work force for the task.
Participation in DOOCS course
Starting of writing of own DOOCS server – client network for the FPGA electronics designed by Elhep.

Near term plans :
Participation in DOOCS development.
Building own DOOCS resources.

9. ELHEP PUBLICATIONS ON TESLA

Several publications are in progress, including conference papers and the next TESLA Technical Reports. The publications summarize our work in progress. These are:(major authors in brackets)

8.1. (TESLA Report) FPGA Internal Interface middleware dedicated for TESLA cavity controller (KP,PR,RR);

8.2. (TESLA Report) FPGA - MatLab middleware layer dedicated for TESLA cavity controller (PR,TCz);

8.3. (TESLA Report) DSP realization in FPGA - initial considerations for TESLA cavity simulator (KP);

8.4. (TESLA Report) FPGA based TESLA cavity simulator TCz,KP,RR);

8.5. (TESLA Report) FPGA based RF Gun controller (TCz,KP,PR);

8.6. (TESLA Report) FPGA behavior in ionizing radiation environment of the TTF (DR,RR);

8.7. (Conference paper) Optoelectronics in TESLA, LHC and pi-of-the-sky experiments (RR,SS); Abstract of this paper is included with this letter;

8.8. (Journal paper) FPGA based LLRF simulation, control and diagnostic system for Tesla, NIM

Three new papers and technical notes are under preparation concerning cavity simulator and controller in MatLab and FPGA/VHDL. 1- DSP procesor; 2-Test set up; 3-Modelling and step connection model in MatLab/FPGA

Three Tesla Reports are considered for publications, being extended versions of prepared papers; http://tesla.desy.de/new_pages/Reports/2003

10. SHORT-TERM PLANS

Time schedules for short term; According to the involved people we have asked the RF Gun will not be in the tunnel with new electronics before several weeks. Thus, perhaps the best time for our next visit is end of November - beginning of December. We may come then possibly for two weeks only if not for shorter period. The VME RF Gun board (basing on the Xilinx trial board, placed inside) should be ready by then.
Planned visits of ELHEP persons and periods of stay
R.Romaniuk – 22 XI – 7 XII
K.Pozniak - 22 XI – 7 XII
W.Zabolotny – 8 days within the period of 22 XI – 7 XII
K.Kierzkowski – 22 XI – 7 XII
T.Czarski – 15 X – 15 XI; 25 XI – 24 XII
P. Rutkowski –
D. Rybka – 15 X – 20 XII
P.Pucyk – 15 X –20 XII
P. Roszkowski – 15 X – 20 XII
T.Jezynski – permanent stay

Immediate tasks
No change yet with respect to the purposes and tasks defined in chapters I-III.
Suggested Plans of ELHEP Group for the nearest future
Pre-next-visit activities (in Warsaw):
Cavity controller and simulator
Further design of simulator
Compillable and synthesizable model of cavity simulator
Hardware for Warsaw ELHEP laboratory needed
New cavity simulator is under consideration, done under pure VHDL. Comparison with MatLab model would then be possible.
Decision on own test board design
The board should consist of:
mother control board – control small Xilinx or Altera chip (Spartan, Acex, Cyclon, etc.)
two daughters boards per one control board - possessing fast Xilinx Virtex or Altera Stratix with DSP modules, and additional components like - SRAM memory, multichannel DAC, ADC, fiber optic Gbit data links, etc, and ETRAX PC.
Full development costs of two test boards at ITR/Warsaw are approx. 5kEuro.
VME crate is needed to test the own development boards

1.3. Next planned visit of ELHEP to TESLA
Suggested visit of a few Elhep members to TTF in September 2003
Tests of cavity simulator
Integration with cavity controller
Preparing Xilinx development boards for tunnel installations, auxiliary equipment, fitting of voltages, supplies, packages, VME crate
Xilinx developments board and software tests
Hardware tests on liniac (XDB).

Option: Laboratory (and on site) tests of own development board

1.4. Following ELHEP visit is planned in November 2003
Predicted tasks:
Tests of PC-VME board.

11. LONG-TERM-PLANS

10.1. Inbuilding of ELHEP into the "online" duties for the TESLA

10.2. Building a mirror ELHEP Laboratory in Warsaw
Such a laboratory will considerably increase the efficiency of the ELHEP Group in DESY. This lab will carry out current hardware work to be implemented in TESLA LLRF control system. The major justification is that ELHEP members (especially senior) stay at DESY only for very confined periods of time. Junior members have to stay in DESY longer to cope with current tasks and to learn the implementation procedures.

Today in the morning I asked very dramatically, once more time, together with TJ, dr Kay Rehlich to exchange one of the small VME crates for a big one. He made responsible for this Mr Olaf Hensler several days ago. Today I will try to write a mail to Mr Hensler, because he seems to be inaccesible in the other way. Perhaps participates all the time in the meetings. I tried to find him several times during a few last days with no result. Perhaps will be lucky today. A big VME crate for Elhep Warsaw is essential (just a minimal condition) for the progress of the work.

Long term tasks and plans

Personal development of ELHEP at DESY
New students and senior experts: Maciej Radtke, Michal Zaczek, Michal Husejko,

Laboratory resources: laboratory space; More permanent laboratory space has to be predicted for ELHEP. Some considerations are necessary how to use this space efficiently, because ELHEP Group members are not always present in DESY.

Laboratory resources: equipment. The Group needs more permanent laboratory hardware set-up. The hardware should include – oscilloscopes, signal generators, a few PCs,

Major directions of electronics development: FPGA, fiber optics, new analog (mixdes) solutions. Consequent shift to own FPGA/VHDL development environment

General directions (and evolution of these) of ELHEP involvement in TESLA and DESY; Especially in view of Tesla Liniac postponing. How does DESY management see the future long term involvement of such a Group like ELHEP?

12. DECISIONS NEEDED

Your decisions are awaited by us in the following matters, what is associated with some costs (real and imaginary), effort, decision pain, hesitation, etc:

10.1. Immediately (this is my strong recommendation) start the work on the backbone MB and some DBs.

10.2. Reworking of the RF Gun controller board. The Xilinx trial board will be placed on a standard VME board with all necessary interfaces added.

10.3. We are still waiting for your decision, either positive or negative, concerning the pieces of equipment to be possibly taken
to the Warsaw ELHEP Lab. The transport chance will expire in three days from now.

10.4. What is your opinion about the short-time-range schedules of the VME RF Gun board implementation near the tunnell?

13. OTHER ACTIVITIES

11.1. Your papers for the Wilga Symp. are very much needed.

11.2. Could you provide me, please, with a reworked list of your publications and cv as we discussed several months ago.

Meetings and tutorials participation in DESY of ELHEP members

7.1. General meetings

1. DESY meeting on future linear collider in the USA, 5-6 June, R.Romaniuk participated
2. Tutorial on DOOCS; ELHEP participants: P.Rutkowski, T.Jezynski, D.Rybka, P.Pucyk, R.Romaniuk, T.Czarski;

Internal meetings

The following meetings were held by the group (TTF Controlroom, bldg. 28, Hall 3):

1. Radiation tests at Liniac II, program document preparation,
2. Preparation of requirements for third generation of LLRF cavity control system using FPGA,
3 Cavity simulator and controller, development stages of FPGA/VHDL Implementation

1. ESGARD Joint Research Program
CARE financed by UE within FP6 (JRP - SRFCAV and SRFTECH); Participation of ISE in ESGARD within DESY group; Waiting for reviewers decisions

2. DESY TESLA contributions to the Proceedings of SPIE, WILGA Symposium 2003

3. IEEE-SPIE WILGA Symposium on Electronics for High Energy Physics Experiments, 21-25 May 2004

4. Dr S.Simrock Visit to IEEE-SPIE ELHEP conference in WILGA on 21-25 May 2003 Invited Paper at IEEE-SPIE sponsored WILGA Symposium on Electronics for High Energy Physics.

5. Video Conference facilities for ELHEP Warsaw Laboratory

Facilitate cooperation between Warsaw Tesla Laboratory and DESY/TESLA
Enable participation of Warsaw ELHEP Laboratory in VC on LLRF&C Systems
The VC was tested between DESY and ELHEP Warsaw and next multiconference additionally with Jefferson Lab, Los Alamos and DESY using ISDN connection.
The problem was Not yet resolved

14. APPENDICES

BMB documentation
Warsaw ELHEP Laboratory status - update for TESLA
Warsaw ELHEP Laboratory status – presentation in CERN for CMS collaboration on 6.6.03

ELHEP visit plans to TESLA during the coming year

ELHEP publications plans

WILGA ELHEP Symposium “Electronics for High Energy Physics Experiments”22-25.05.03
Meetings
Conf. On Radiation Hardness of Semiconductor Detectors

Administrative documents

Protokoll zur Strahlenschutz-Unterweisung for ELHEP members
Tutorial on radiation safety in LINIAC II
DESY Invitations for ELHEP members
Personal DESY documents for International Office