Warsaw ELHEP Group

Research Visit Summary at DESY, TESLA

17.November – 01 December 2002

Warsaw University of Technology
Institute of Electronic Systems

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DESY, 27 November 2002

ELHEP Structure
For Xilinx/Altera test boards task

1. THEORY Layer:
tasks – mastering of basic model of cavity; seeking for optimal and new cavity models, checking simulations;
people - TC-coordinator, WZ,TJ, RR

2. MATLAB & DSP Layer:
tasks – performing cavity simulator and controller, combining simulator and controller;
people – WZ-coordinator; WZ does controller and simple simulator, TC,RR support from theoretical side, TJ supports from practical side;

3. PURE VHDL Layer:
tasks – full system implementation in VHDL
Results of WZ+TC+TJ are implemented in VHDL environment by KTP and MK.
Functionalities: Internal Interface (Communication with physical device); Control, Diagnostic, Monitoring, Exceptions handling;
Communication with the board via USB: AB, TJ
people – KP-coordinator, MK, TJ,

4. SOFTWARE Layer:
tasks -
Software for communication with the board in Borland C++: PR, MP, TJ, Board control;
Software for functionalities service: controller and simulator;
Board user interface: PR, KK, MK., Software analysis; TC;
people – PR-coordinator (future), MP, TJ, KK, MK,

5. LABORATORY Layer:
tasks - Laboratory infrastructure: measurements, signal observations, hardware diagnostic and monitoring, hardware setup, Laboratory Hardware stand
people – all ELHEP members

6. ANALYSIS Layer
tasks - Feedback between theory, model and measurements
people – TC, WZ, KP, RR

Addendum: *Works under current realization*

1. THEORY Layer:
- realization of Matlab model of the cavity, consideration of mechanical and other effects

2. MATLAB & DSP Layer:
- realization of the prototype of a simple simulator model, (three variants realized, differing structurally)
- analysis of model efficiency – clock, chip occupancy,

3. PURE VHDL Layer:
implementation of Internal Interface with USB interface
implementation of Internal Interface with model of controller
implementation of Internal Interface with model of simulator

4. SOFTWARE Layer:
controller module for all Xilinx board functionalities
steering of cavity controller hardware application based on Matlab core and Internal Interface
steering of cavity simulator hardware application based on Matlab core and Internal Interface

5. LABORATORY Layer:
realized initial laboratory set up basing on modest borrowed equipment

6. ANALYSIS Layer
not yet available

Plans for next steps

1. THEORY Layer:
Models of cavity (by TC) must be modified for requirements imposed by the DSP
Continuation of theoretical models

2. MATLAB & DSP Layer:
Realization of more effective models of controller and simulator
Realization of models for Altera/Stratix

3. PURE VHDL Layer:
Addition of diagnostics, monitoring and exception handling functionalities to the Matlab&DSP models of cavity controller and cavity simulator
Realization of hardware models based on Altera/Stratix test board

4. SOFTWARE Layer:
Application of hardware functionalities (diagnostics, monitoring, exception handling)
Software analysis of hardware work quality
Realization of steering for Altera/Stratix test board

5. LABORATORY Layer:
Very important!! Full test stand should be assembled and performed

6. ANALYSIS Layer
Beginning, System verification, Comparison of results between all layers

Laboratory apparatus

Oscilloscope – Tektronix 700 or 7000 with probe, 2GHz, - price around 35kEuro
Small test oscilloscope – Tektronics 3000 series, 500 MHz, 5 GS/s, - price 9kEuro
Small test oscilloscope – Tektronix 220 - price around 3.kEuro
Pulse Generator Agilent, 150 MHz, - price around 9kEuro
Function Generator - 80 MHz, - price around 4,5kEuro
Function Generator Agilent 15 MHz, - price 2kEuro
Multi-voltage HAMEG Power Supply Units – 3 pieces, - price around 2kEuro for all,
VME crate 6HE, two pieces, with Controller BIT3/PC, - price around 2x8kEuro=16kEuro
Measurement standard converter CAN, GPIB, RS, ETH, - two pieces – 2x2kEuro=4kEuro
Precision Soldering Station - 2 pieces 2x400Euro, price around 1kEuro

From the above equipment to Warsaw laboratory
Tektronix 3000
Function generator
Multi-voltage supply unit, 1 piece
VME crate 6HE with Controller BIT3/PC – 1 piece
Measurement standards converter – 1 piece
Precision soldering station – 1 piece

JUSTIFICATION of apparatus at DESY
2GHz scope needed permanently for basic measurements of 100MHz square wave signals and precise measurements of time shifts, distortions, etc.
Small scope is needed for students work, learning, coarse testing, etc.
Pulse generator is necessary for clocking of digital chips (clock forming, clock shift, frequency synthesis).
Function generator is necessary to simulate input analog signals.
VME crate with controller is necessary for building of prototypes.
Converters serve for steering and connection between various commercial measurement equipment.

JUSTIFICATION of apparatus for ELHEP Warsaw Laboratory
Warsaw laboratory serves for work preparing to be implemented in DESY.
Small scope for Warsaw is designed for down scaled replacement of 2GHz.
Modest version of function generator to simulate input analog signals
Justification of the rest of apparatus as above.

Software
ISE XILINX 5.1. licence, price around 1kEuro (for education)
Borland C++ Programming Environment Java Builder 7 – price around 2kEuro
Matlab DSP core Generator for Altera, price around 2kEuro

Agreement on Joint Projects between DESY and Warsaw University of Technology

Appendix to Annex 1

This appendix is a specification of costs for the whole year 2003

Expenses for Manpower

Six positions expenses for manpower are planned (Postdoctoral fellow, research & development, associate coordinator, Ph.D. students, all working at DESY)

Expenses for travel and hardware

Approximately 65 visits of the collaboration members from ISE are planned to DESY. The travel expenses will be managed by DESY (total travel costs c.a. 10.000 Euro)

DESY will cover costs of their stay at the facility according to DESY regulations.

Costs of components for prototyping (1.01.-31.12.2003)

The components will be procured by DESY.

1. Design of the low level rf control system for TTF phase II (office equipment, PC's, 10.000 Euro)
2. Prototyping and performance evaluation of LLRF sub-system 40.000 Euro

Total components ca. 50.000 Euro

Signatures

Dr D.Trines
DESY

Hamburg, ……..

Prof. J.A.Dobrowolski
ISE PW

Warsaw, ……..

List of Warsaw ELHEP Group members, subject to visits in 2003

Long term visits:

Tomasz Jezynski – one year (continuation)
Tomasz Czarski – one year; three visits per one month, one visit per half year (4)
Piotr Rutkowski – one year (2)
Krzysztof Czuba (prof. J.Dobrowolski)– one year (1)
Seweryn Jodlowski – half year (1)
Waldemar Koprek – half year (1)

Short term visits:

Krzysztof Pozniak – 5 times per two-weeks, 2 times per three weeks (7 visits)
Ryszard Romaniuk – 5 times per two weeks, 2 times per three weeks (7)
Krzysztof Kierzkowski – 5 times per two weeks, 2 times per three weeks (7)
Maciej Kudla – 5 times per one two weeks, 2 times per three weeks (7)
Janusz Dobrowolski – 2 times per one week (2)
Wojciech Zabolotny – 6 times per two weeks (6)
Mariusz Ptak – 2 times 3 weeks (2)
Karol Bunkowski – 3 times per two weeks (3)
Michal Pietrusinski – 5 times per two weeks, 2 times per three weeks (7)
Waldemar Koprek – 2 times per 6 weeks two months during vacation (3)
Adam Grodecki – 2 times per 6 weeks two months during vacation (3)
Seweryn Jodlowski – 2 times six weeks (2)

Total predicted number of visits: 65
Reserve 5 ?
Travel expenses 65 x 150 Euro = 9750 Euro
Total travel expenses 10kEuro

Key to names: MP-Michal Pietrusinski, KP-Krzysztof Pozniak, KK-Krzysztof Kierzkowski, MK-Maciej Kudla, WZ-Wojciech Zabolotny, PR-Piotr Rutkowski, TJ-Tomasz Jezynski, TG-Tomasz Czarski, RR-Ryszard Romaniuk,