RF_Controller - FPGA trial

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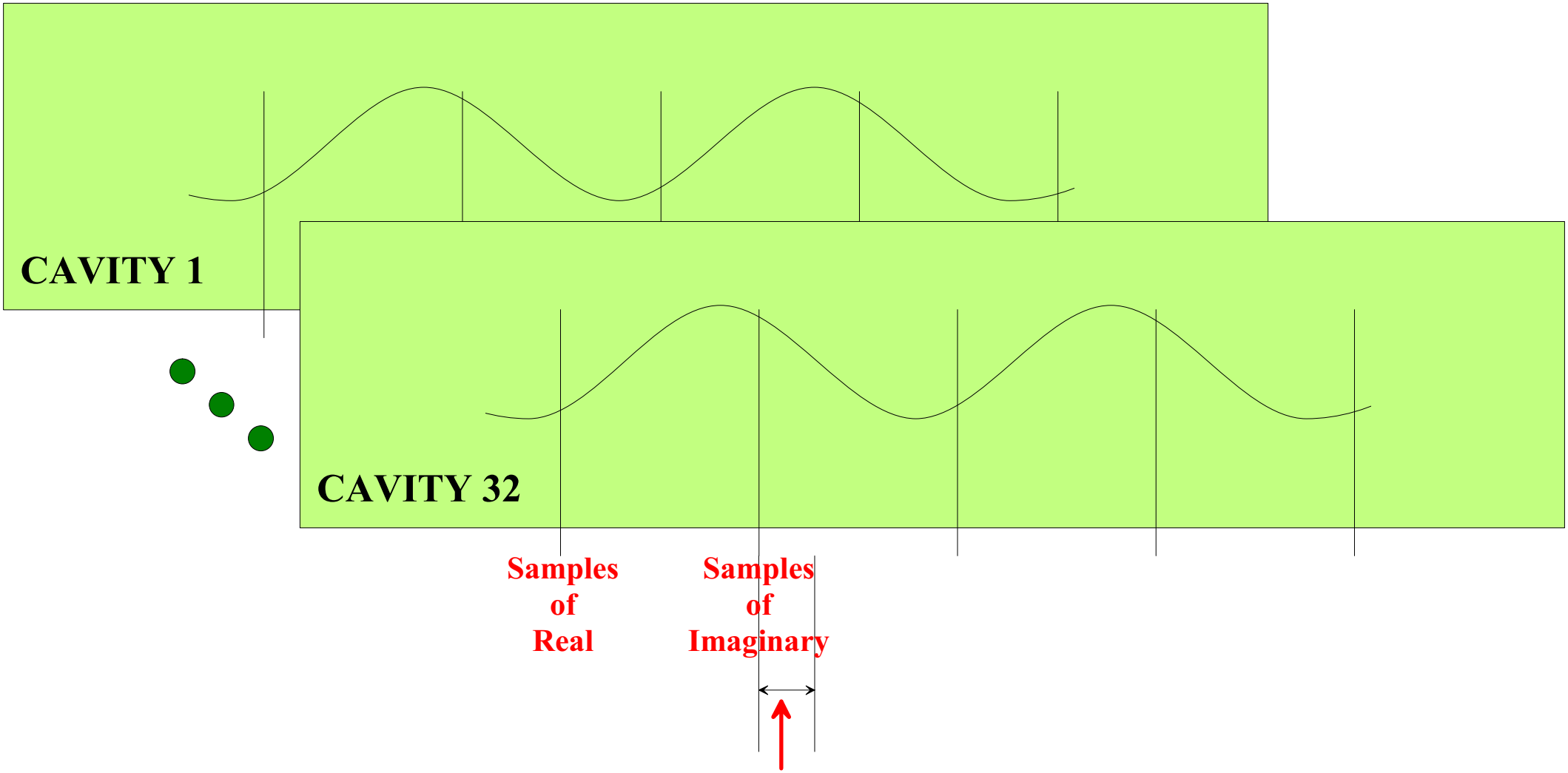
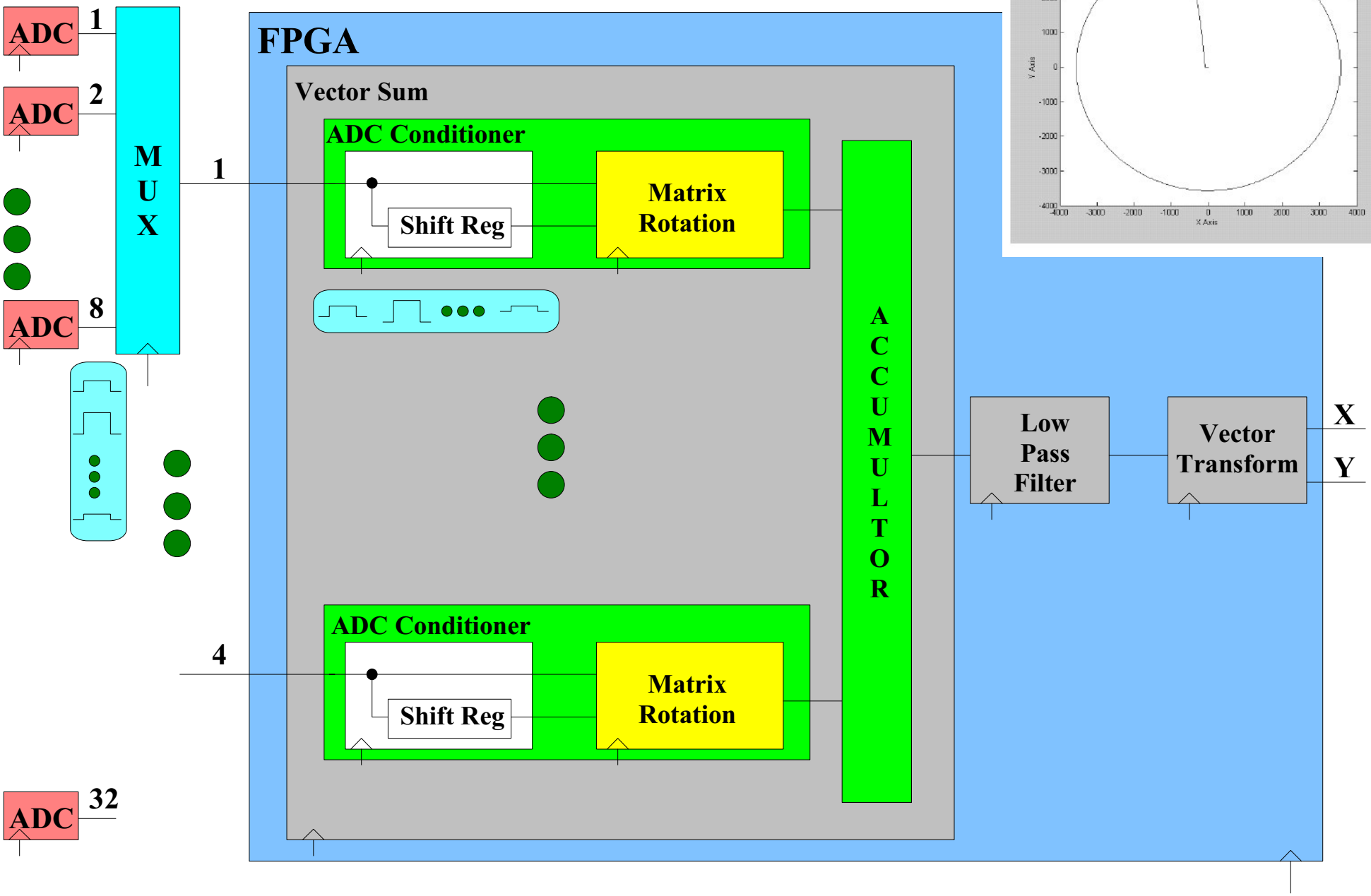
LLRF meeting - September 19, 2002

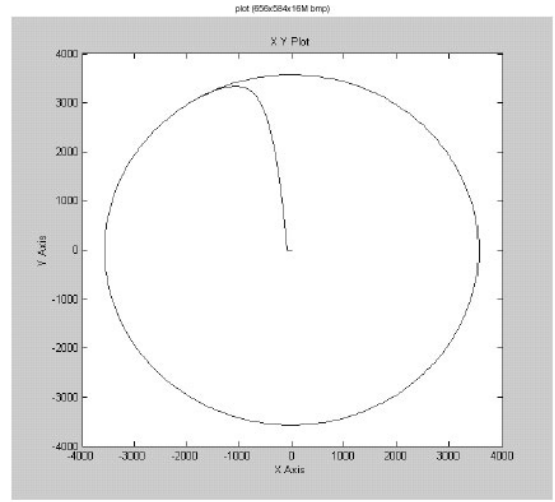
RF_Controller - where is located

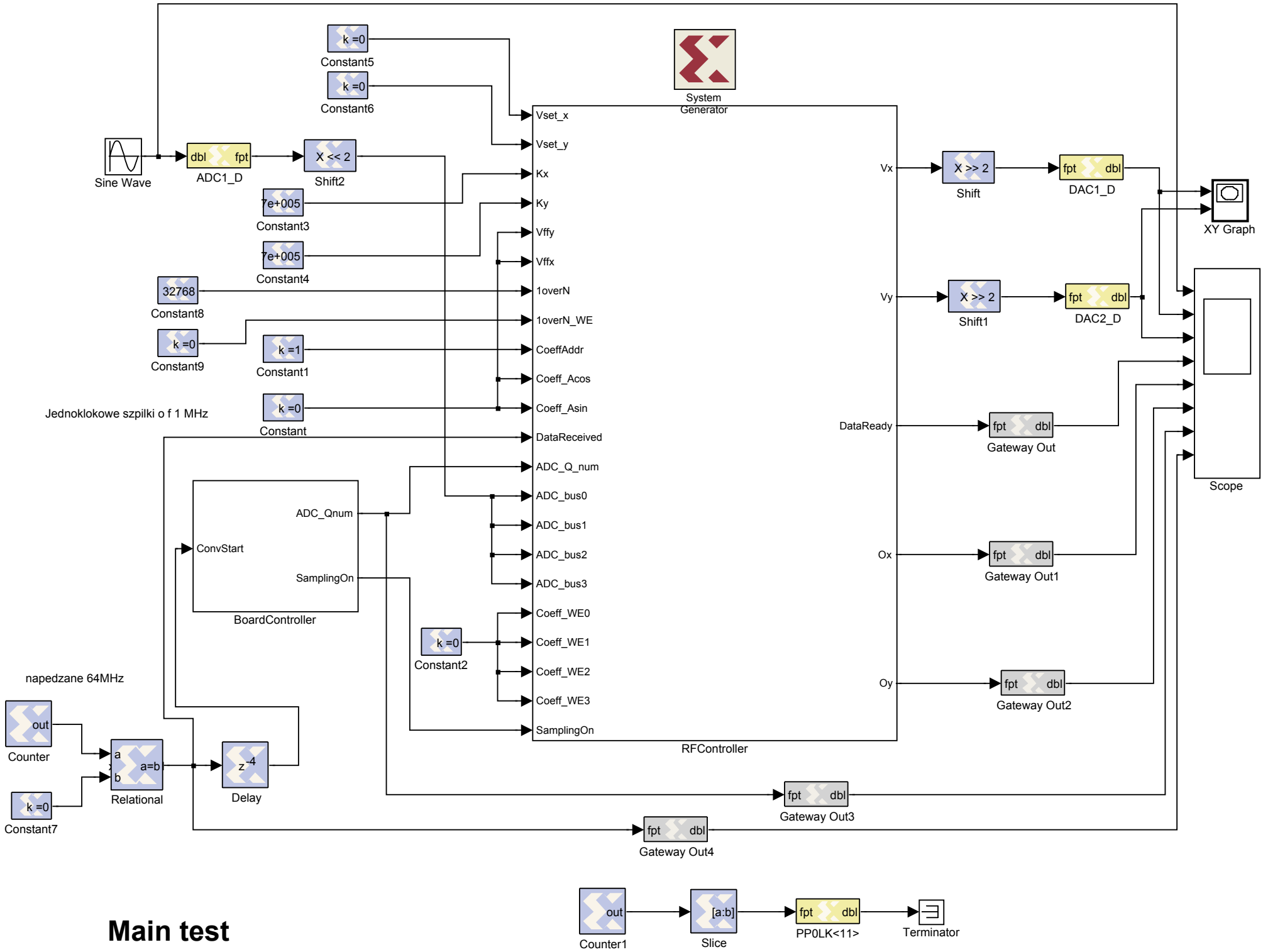


Rf_ConTroller is pipelined device with clock equal to the clock of ADC and multiplexing of ADC data

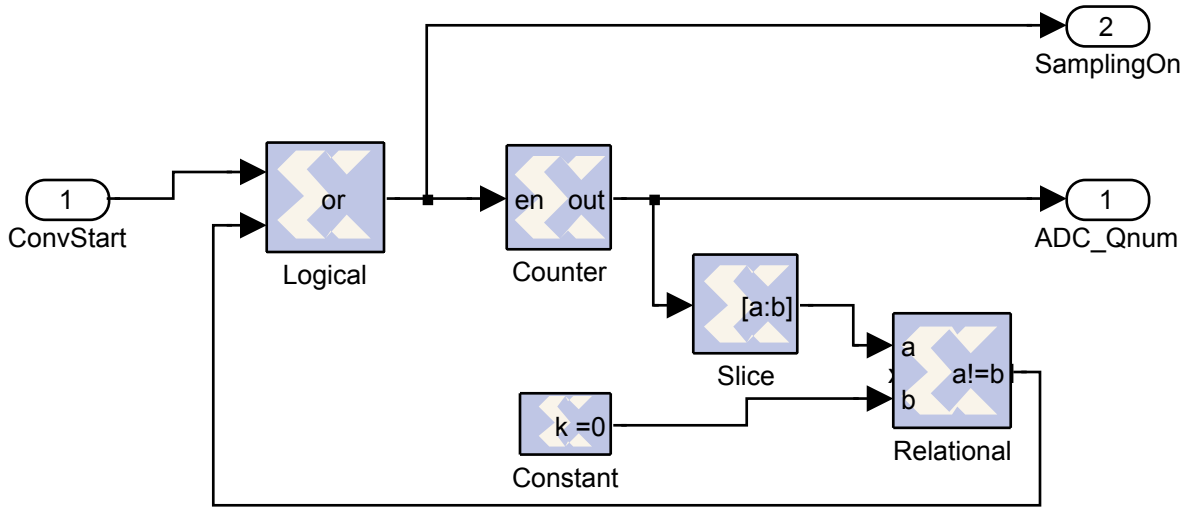
RF_Controller - how it is constructed



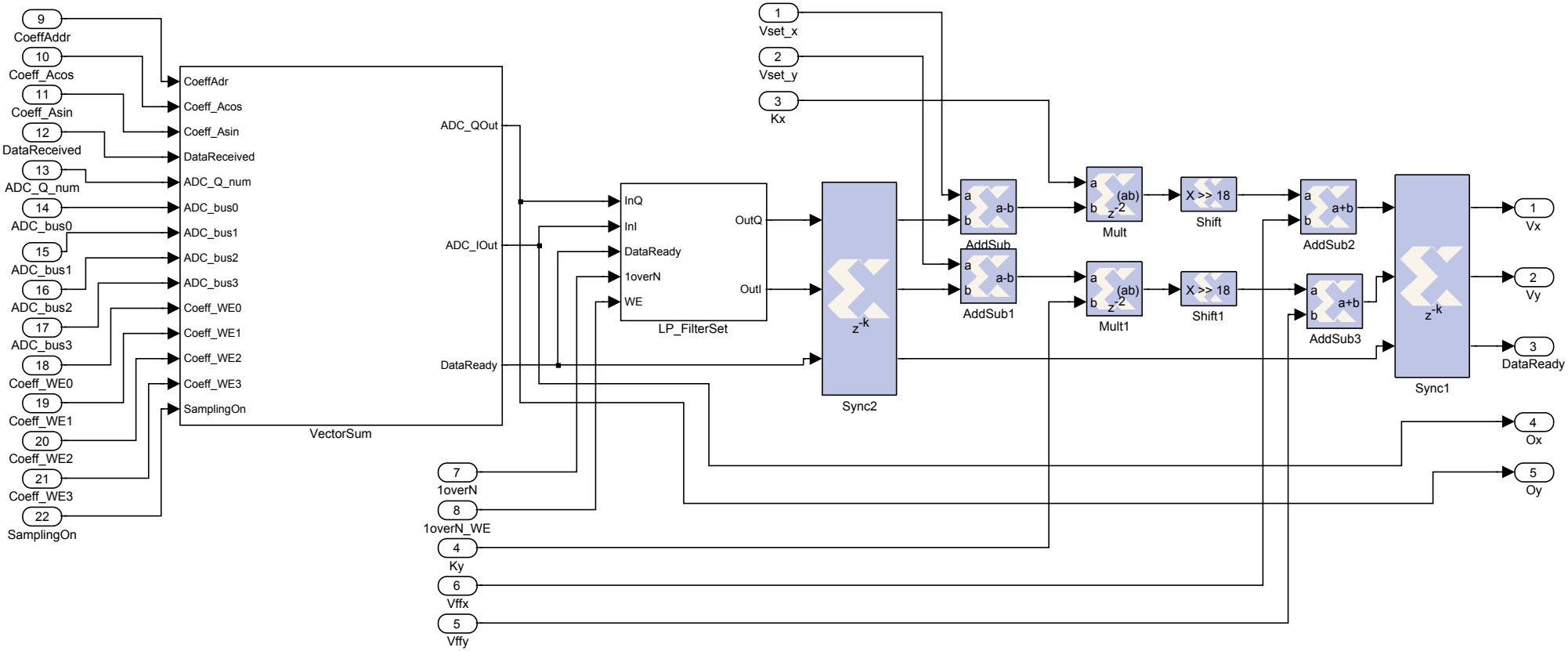



Constant5
k =0
Constant6
k =0
System Generator
Sine Wave
dbl
fpt
ADC1_D
X << 2
Shift2
7e+005
Constant3
7e+005
Constant4
32768
Constant8
k =0
Constant9
k =1
Constant1
Jednoklokowe szpilki o f 1 MHz
k =0
Constant
Vset_x
Vset_y
Kx
Ky
Vffy
Vffx
1overN
1overN_WE
CoeffAddr
Coeff_Acos
Coeff_Asin
DataReceived
ADC_Q_num
ADC_bus0
ADC_bus1
ADC_bus2
ADC_bus3
Coeff_WE0
Coeff_WE1
Coeff_WE2
Coeff_WE3
SamplingOn
RFController
Vx
Vy
DataReady
Ox
Oy
X >> 2
Shift
X >> 2
Shift1
DAC1_D
DAC2_D
Gateway Out
Gateway Out1
Gateway Out2
XY Graph
Scope
ADC_Qnum
ConvStart
SamplingOn
BoardController
k =0
Constant2
napedzane 64MHz
out
Counter
k =0
Constant7
a
b
a=b
Relational
z -4
Delay
Gateway Out3
Gateway Out4
out
Counter1
[a:b]
Slice
PP0LK<11>
Terminator

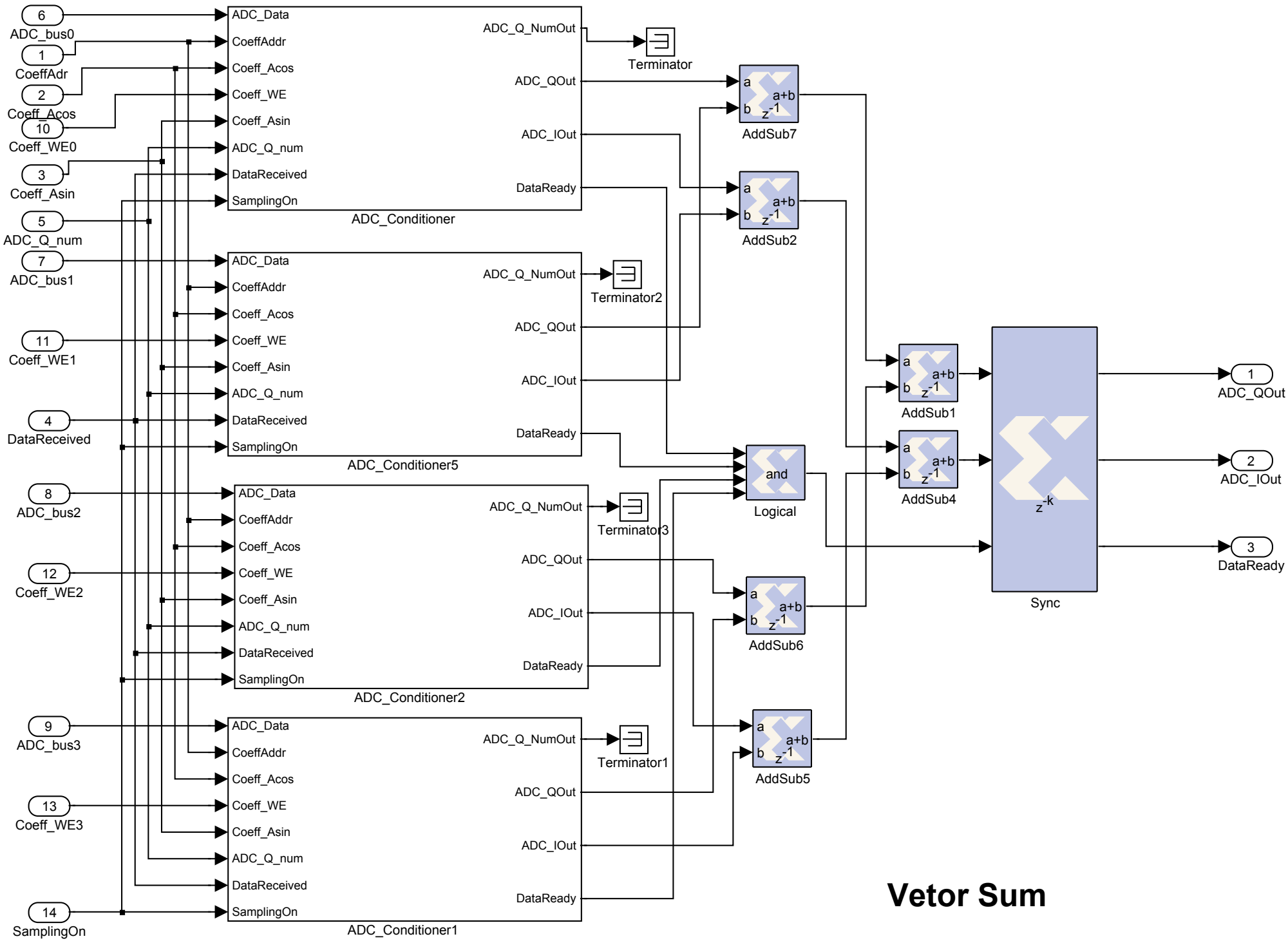
Main test



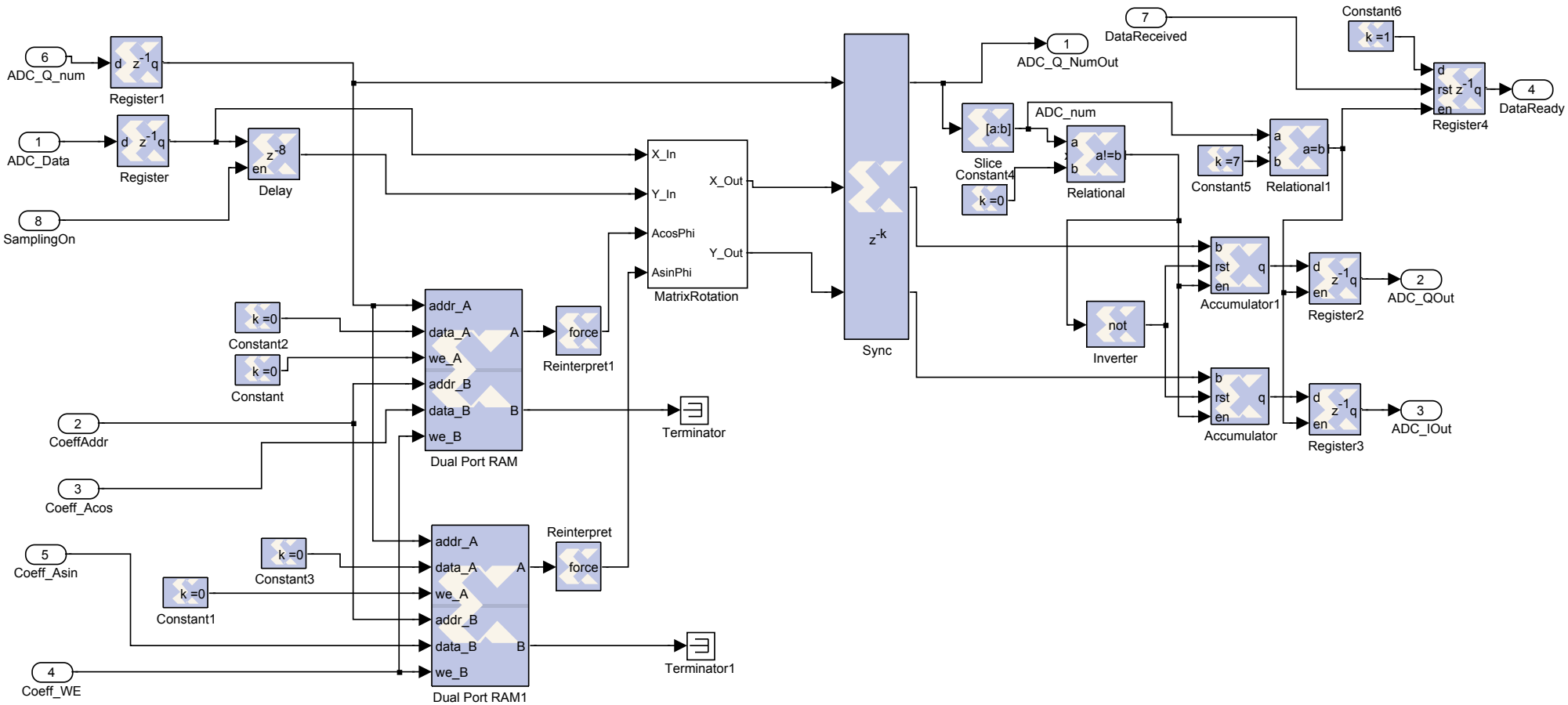
Board Controller



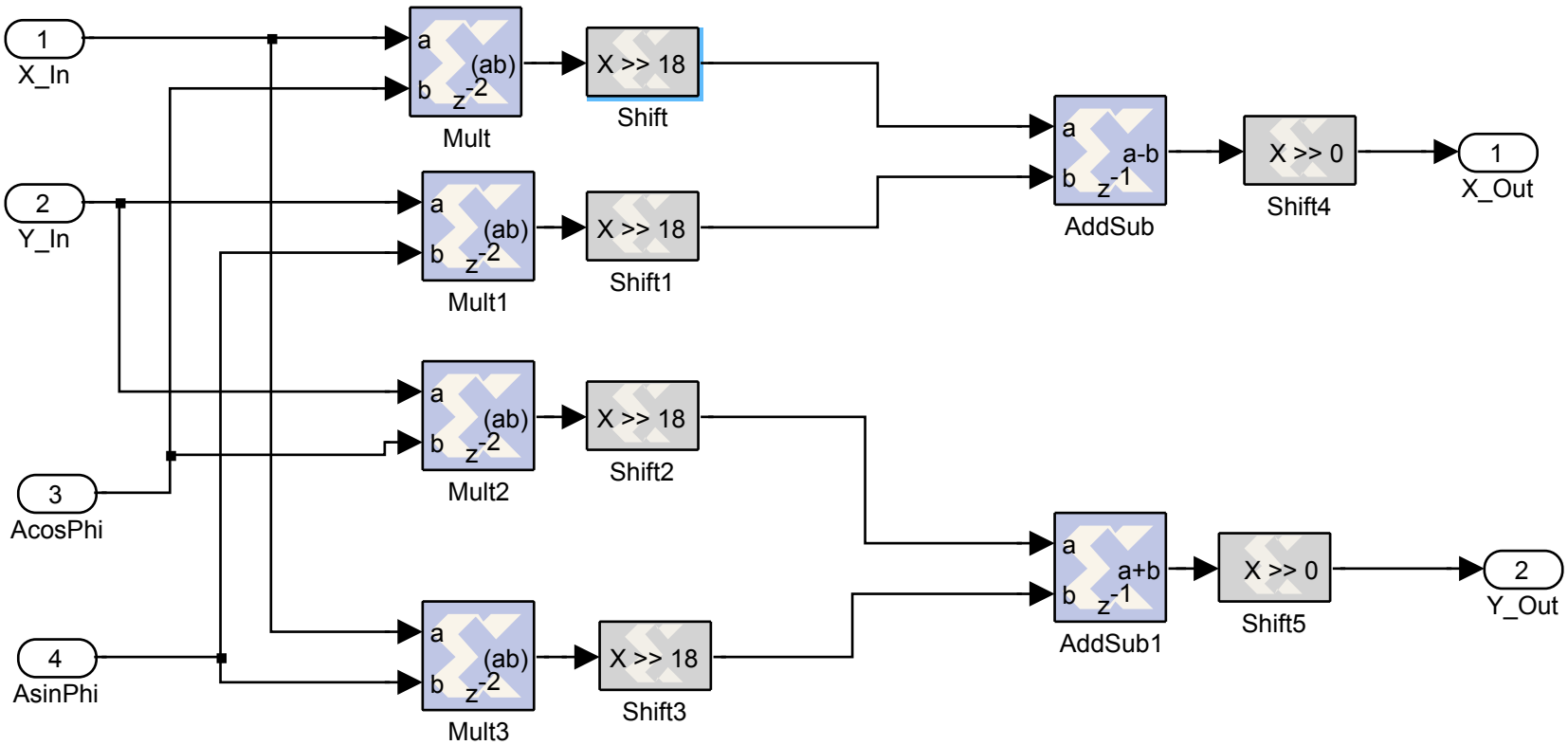
RF Controller


6
ADC_bus0
1
CoeffAdr
2
Coeff_Acos
10
Coeff_WE0
3
Coeff_Asin
5
ADC_Q_num
7
ADC_bus1
11
Coeff_WE1
4
DataReceived
8
ADC_bus2
12
Coeff_WE2
9
ADC_bus3
13
Coeff_WE3
14
SamplingOn
ADC_Data
CoeffAddr
Coeff_Acos
Coeff_WE
Coeff_Asin
ADC_Q_num
DataReceived
SamplingOn
ADC_Q_NumOut
ADC_QOut
ADC_IOut
DataReady
ADC_Conditioner
ADC_Conditioner5
ADC_Conditioner2
ADC_Conditioner1
Terminator
Terminator2
Terminator3
Terminator1
AddSub7
AddSub2
AddSub1
AddSub4
AddSub6
AddSub5
Logical
and
Sync
1
ADC_QOut
2
ADC_IOut
3
DataReady

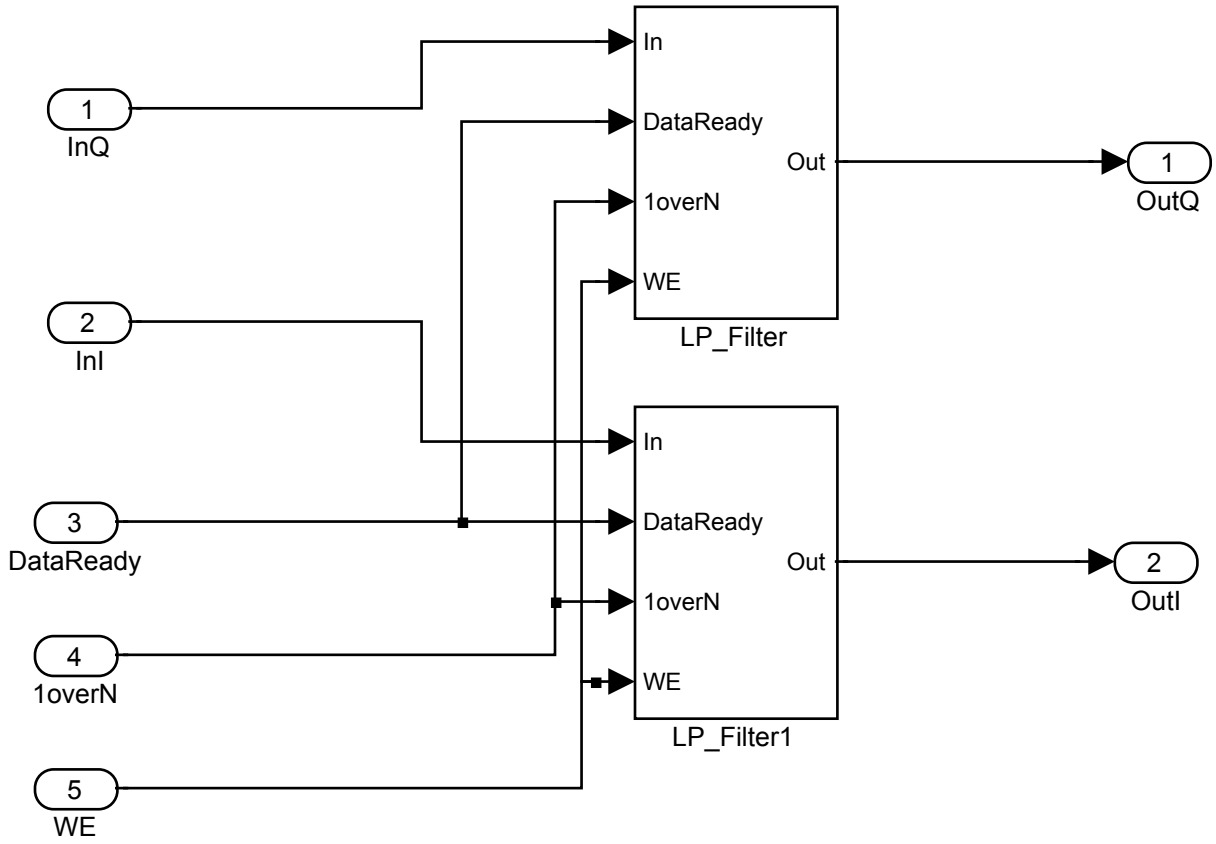
Vetor Sum



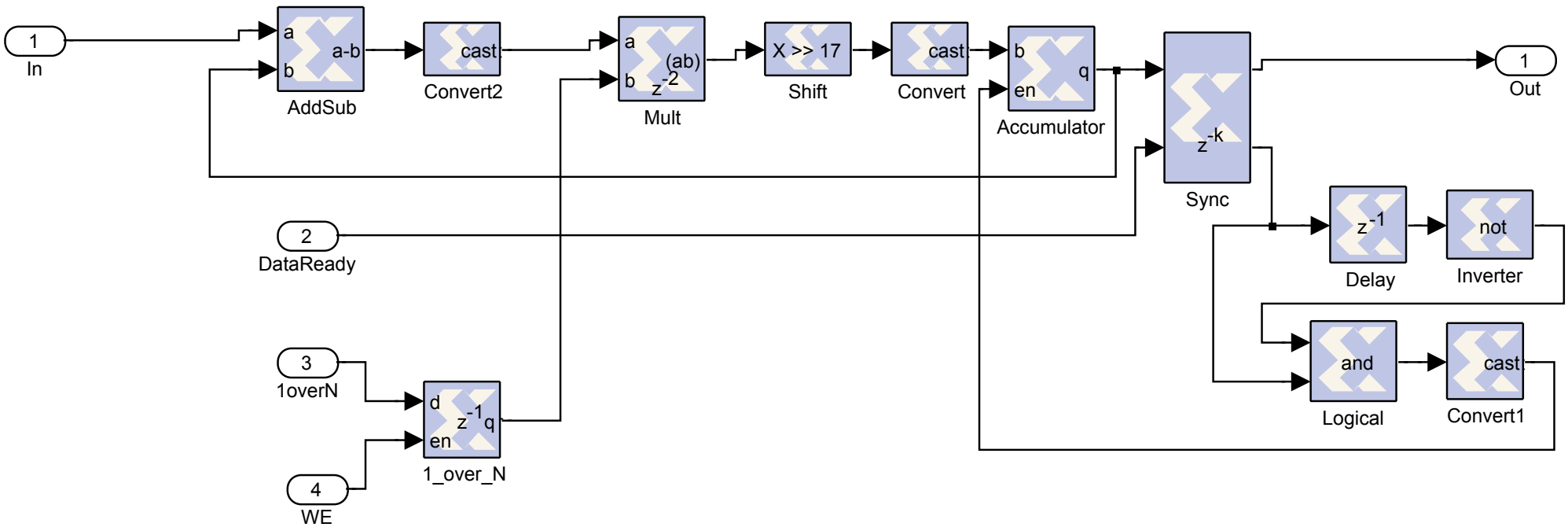
ADC Conditioner



Matrix Rotation

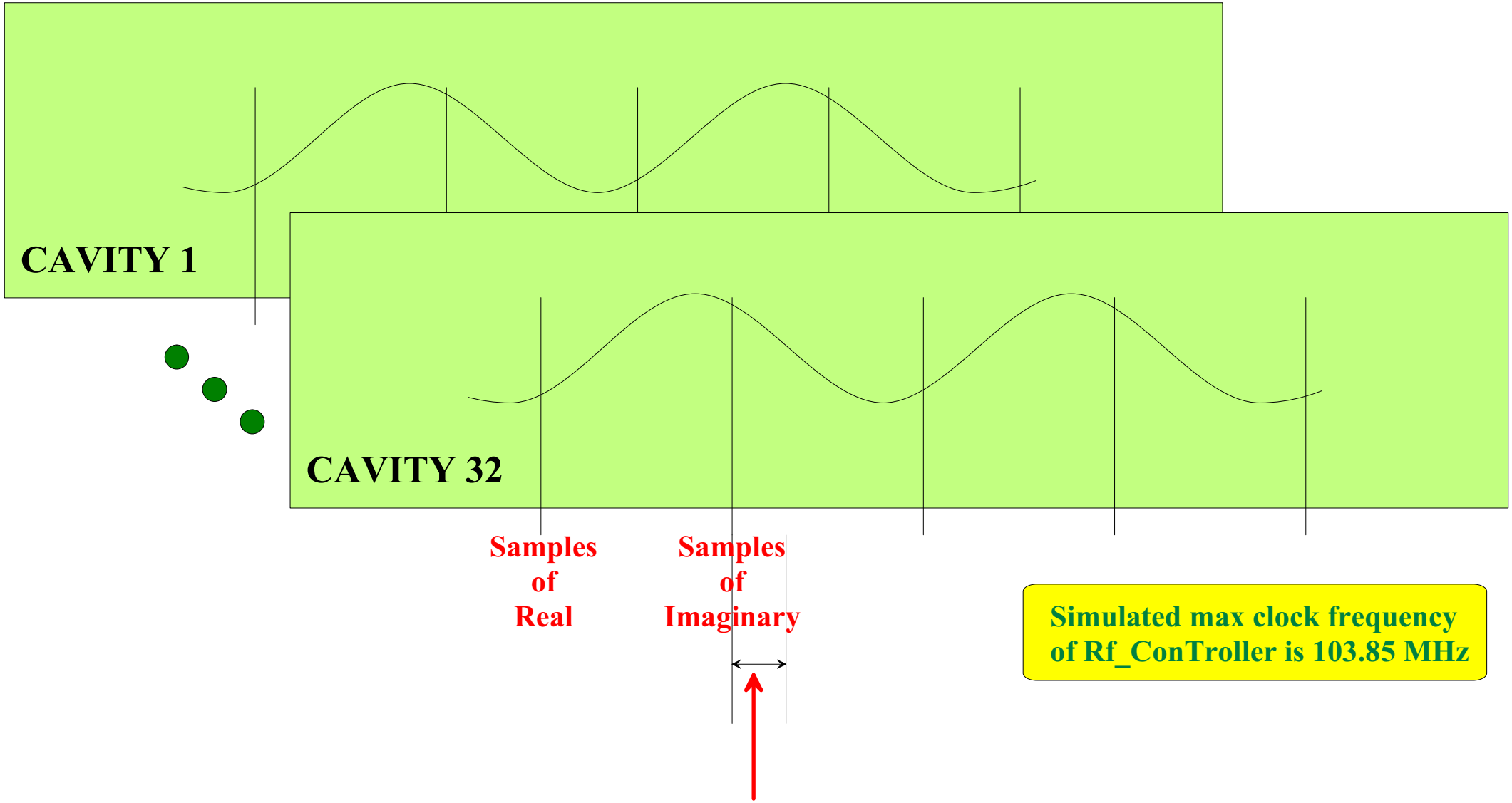


LP Filter Set


1
In
a
b
a-b
AddSub
cast
Convert2
a
b
(ab)
z-2
Mult
X >> 17
Shift
cast
Convert
b
en
q
Accumulator
z-k
Sync
1
Out
2
DataReady
z-1
Delay
not
Inverter
3
1overN
d
z-1
q
en
1_over_N
4
WE
and
Logical
cast
Convert1

LP Filter

RF_Controller - what is its performance

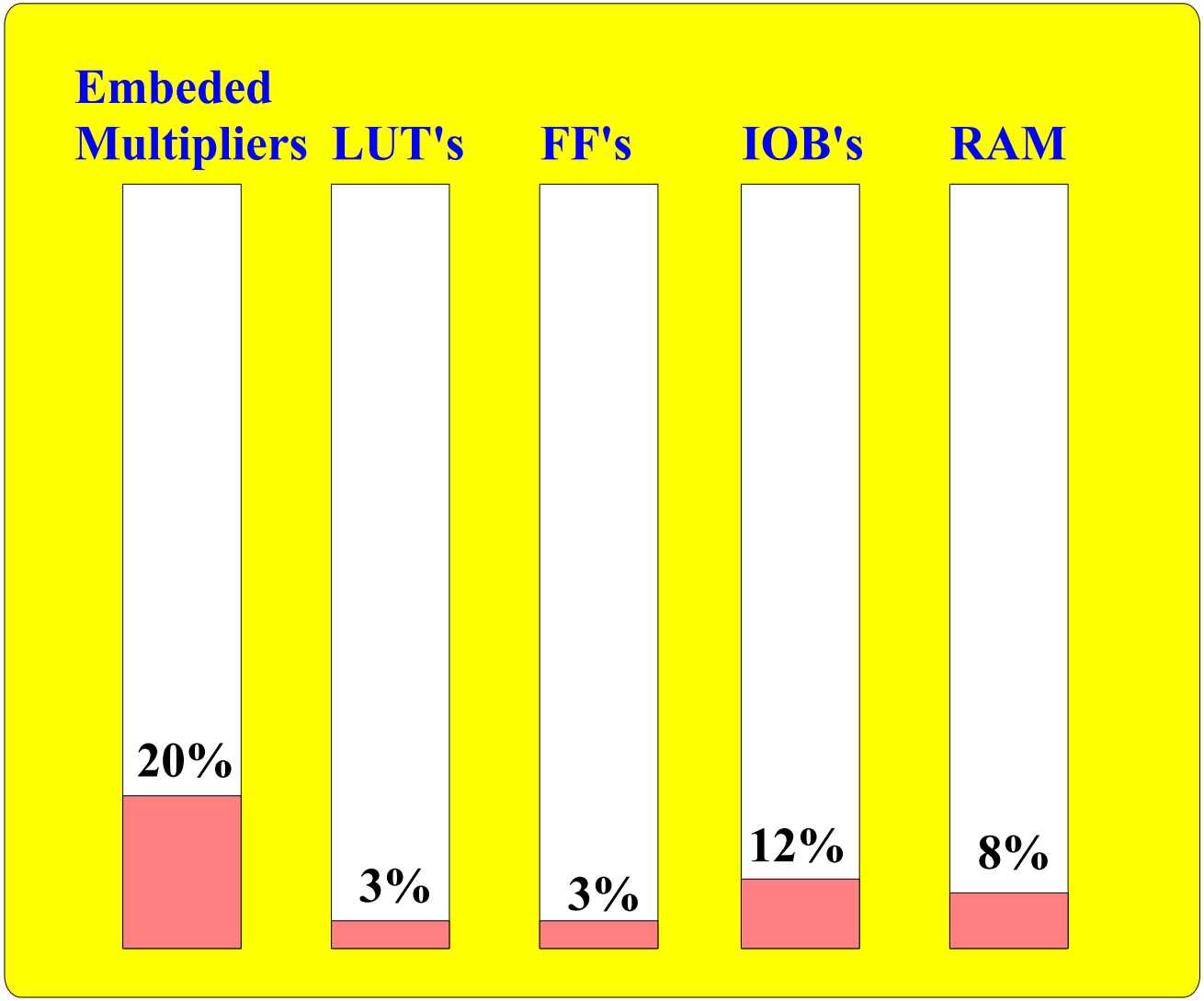


Simulated max clock frequency of Rf_ConTroller is 103.85 MHz

LATENCY = ADC_Latency + Converter_Number + Rf_CTrl_Latency =
3 + 8 + 8 = 19 periods
= 320 ns (if clock freq, is 64 MHz)

RF_Controller - what part of FPGA's resources are used

(Xilinx demo board contains Virtex II - 3000)



Summary

FPGA can do fast pipelined matrix rotation, low pass filter, matrix transformation for rf control with clock ~100 MHZ and latency of 10 periods, very small resource occupancy in case of XC2V3000;

system vue of the control to be defined (data acquisition, control & monitoring, interfacing);

other control (slope of decay phase, Kalman, etc...) tasks should be defined and verified;

VHDL description versus Matlab to be evaluated;

usage of embedded processor to be evaluated (some task should be done there);

other FPGA (Stratix) to be evaluated.