LLRF-ATCA
LOW LEVEL APPLICATIONS

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AGENDA

1. ATCA architecture for low level applications
   requirements, architecture, communication, scalability
2. ATCA motherboard for low level applications
   architecture, resources, communication
3. Multiprocessor computation and distribution of algorithms
4. Review of current algorithms
5. Future algorithm development
6. Experimental results

ATCA architecture for low level applications

Requirements for LLRF System:

- Total length of the facility: 3.4 km, Accelerator tunnel: 2.1km, Depth underground: 6 - 38 meters
- Wavelength of X-ray radiation: 6 to 0.085 nm
- ~1000 s.c. cavities (1.3 GHz), 30 RF station 30MV/m(10 MW klystron)
- Required field stability : 10-5 in amplitude, 0.01° in phase
- Continuous operation is required: only one maintenance day per month

Advantages:

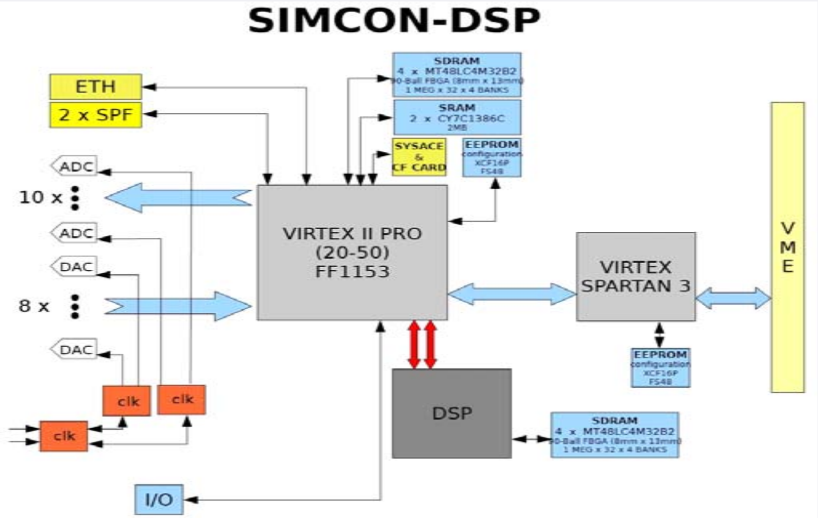
Scalable / Flexible (modularity - partially upgradeable, add new, not know during design, functionality)

- Reliable / Redundant (VM, timing, power, etc...)
- Fast and high resolution inputs, > 100 inp. a. ch. / RF St.
- Low latency (fast communication links)
- Support modern control algorithms
- Reliability, operability and maintainability

VME SIMCON-DSP

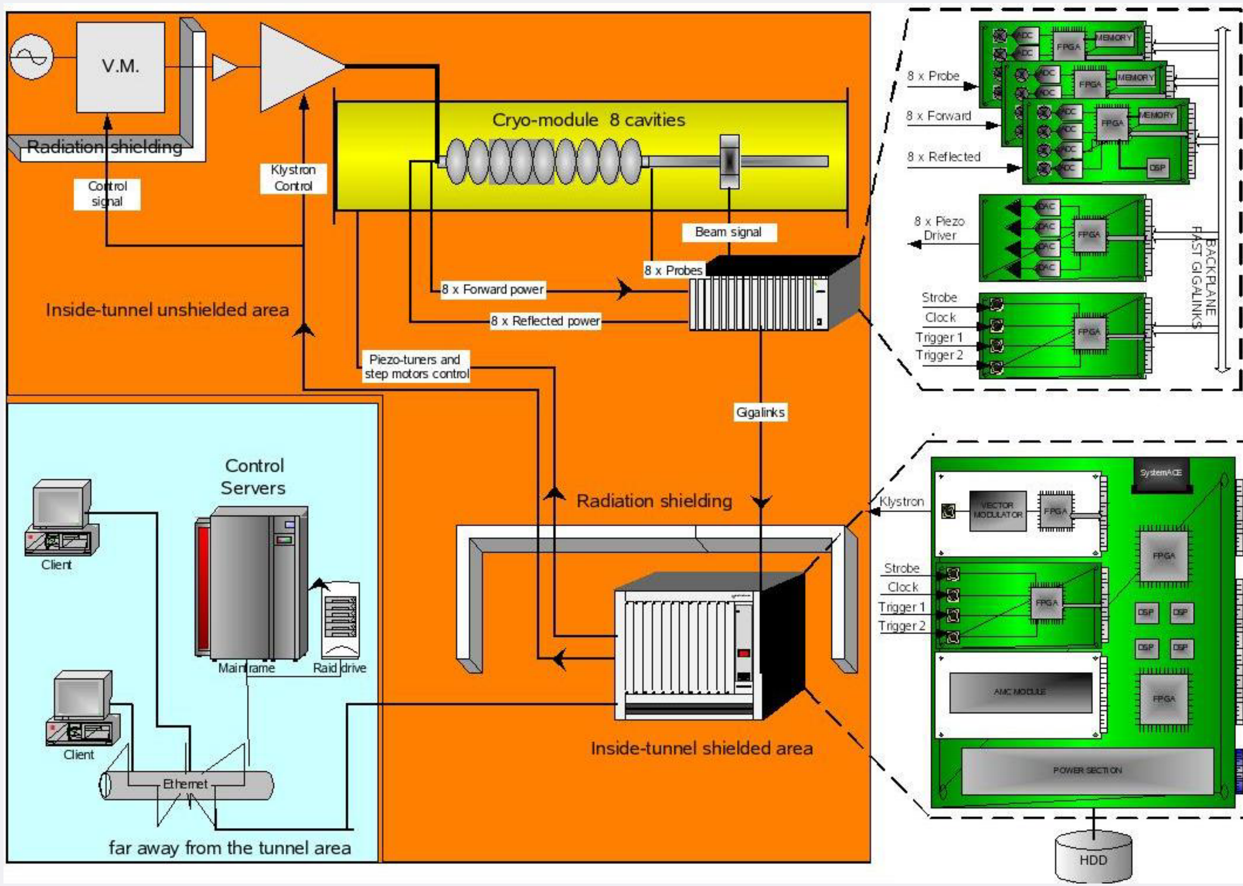
Limits of current architecture:

- Communications: ☹
- One FPGA chip for cavity contorller and system communications
- Slow VME bus communication
- Limits for number of I/O signals
- No dual CPU VME boards for support



ATCA architecture for low level applications

- Architecture
- Communication
- Scalability



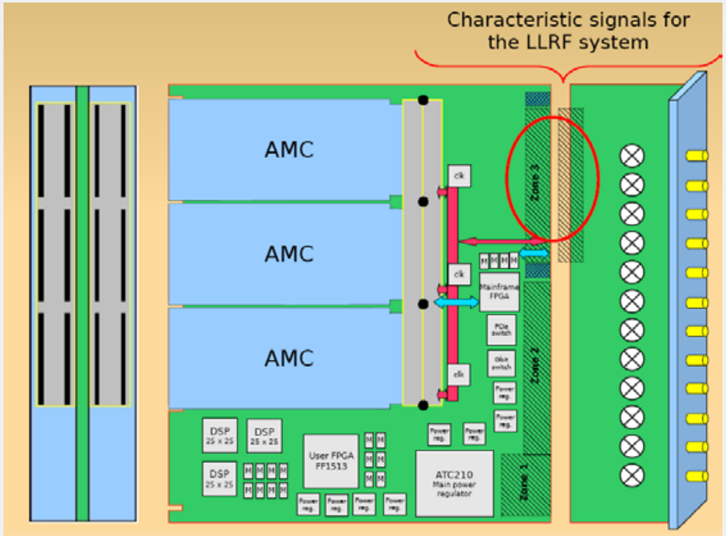
LLRF-ATCA STANDARD

ATCA and AMC Boards:

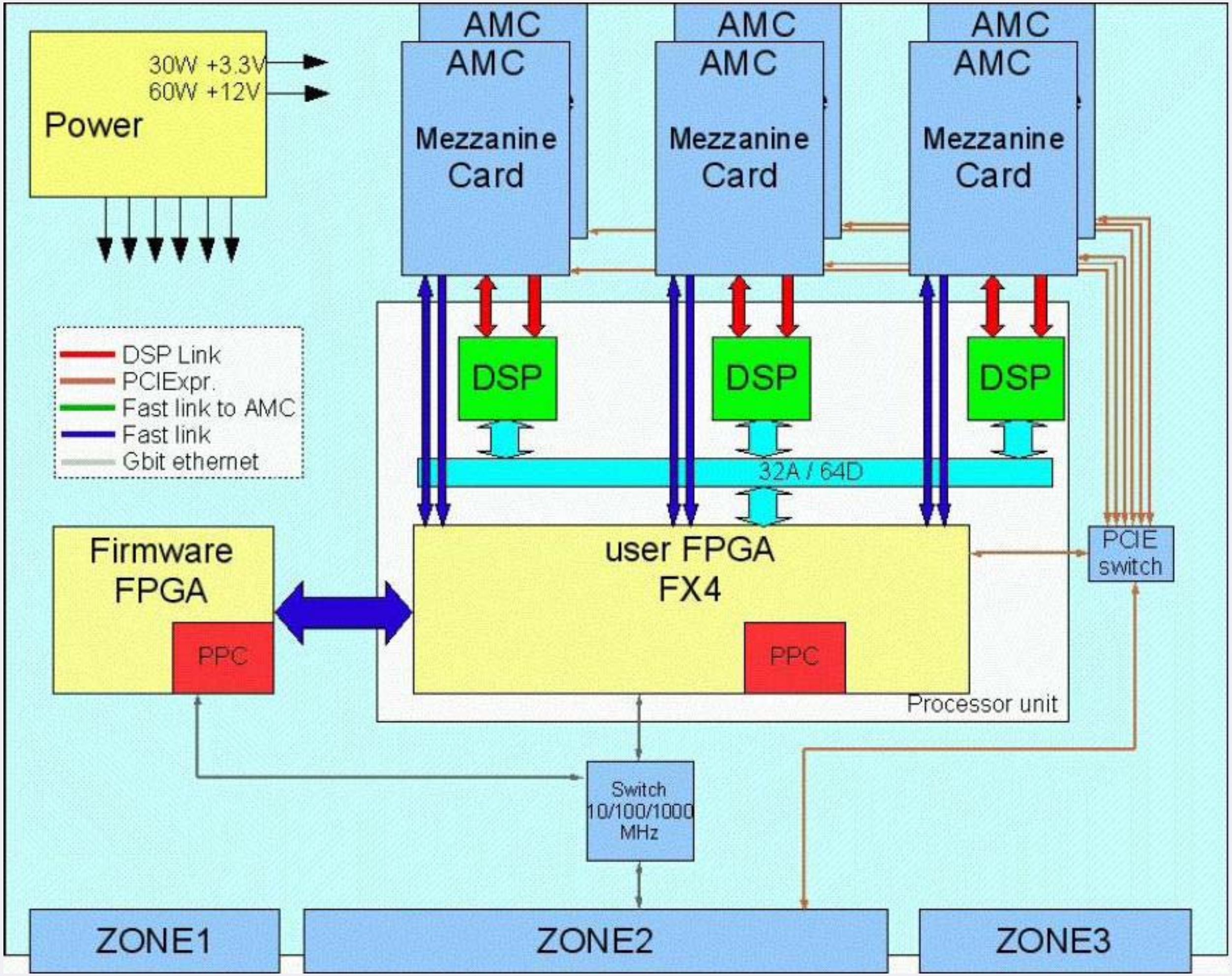
- AMC module 8xADC + FPGA (100MHz)
- AMC Vector Modulator + 2xDAC (800MHz) + memory + FPGA
- AMC Vector Modulator + 1xDAC (1600MHz) + memory
- AMC module Timming receiver (Trigger) + clock synthezer
- AMC Piezo Sensors
- AMC Transient Detections
- AMC module 64 ch. digital IO
- AMC for signal processing (FPGA, DSP)
- AMC module 32 ch. slow analog I/O (1MHz)
- AMC stepper motor controller
- RF Reference receiver and distribution

Easy system upgrade -> new AMC boards -> new functionality

Communication to AMC boards



LLRF-ATCA Board



LLRF-ATCA Board

Communications:

GigaBit Ethernet

PCI-E

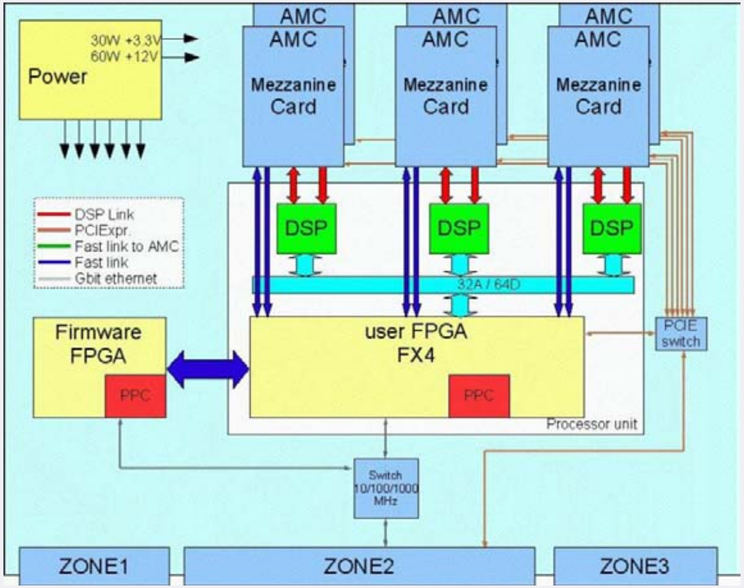
DLinks

DSP-DSP bus

User-Defined Protocols
FPGA-FPGA,
FPGA-AMC

Resources:

- FPGA
- 3 x DSP TS201
- Easy upgrade via specialized AMC cards !!!



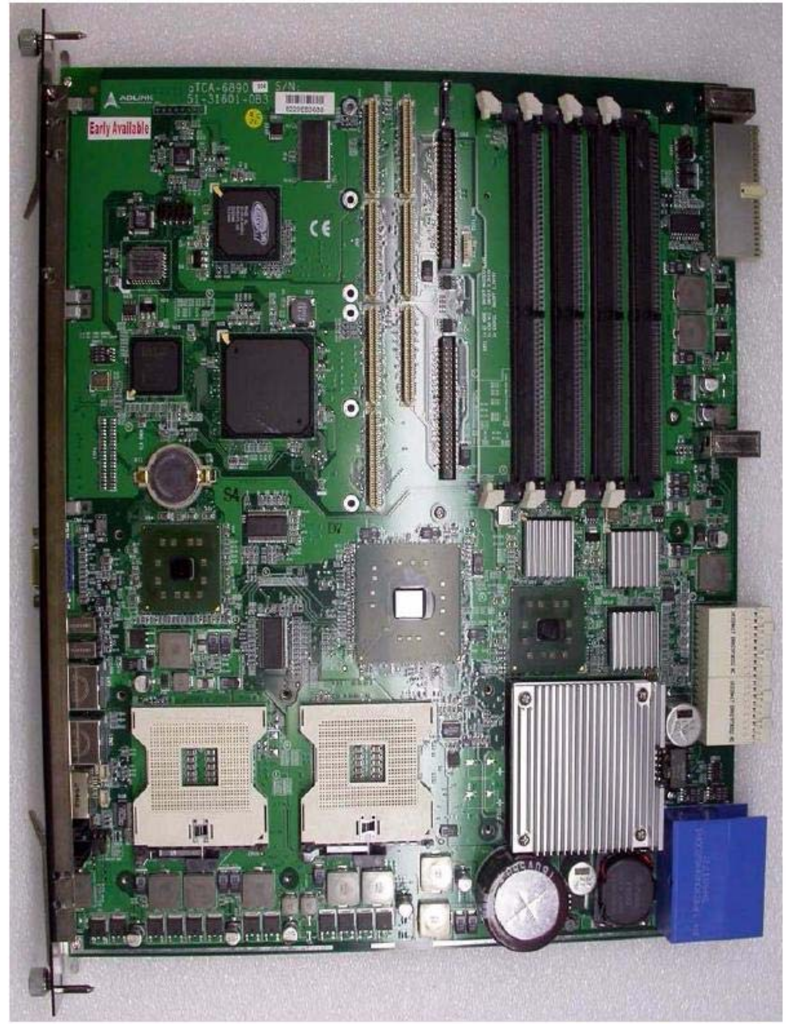
Multiprocessor Computation

Multiprocessor computation and distribution of algorithms

Cluster of Dual CPU Intel Processors Unit (ADLINK CPU-6890 board)

Fast GigaBit Ethernet on backplane

Up to 8 Boards

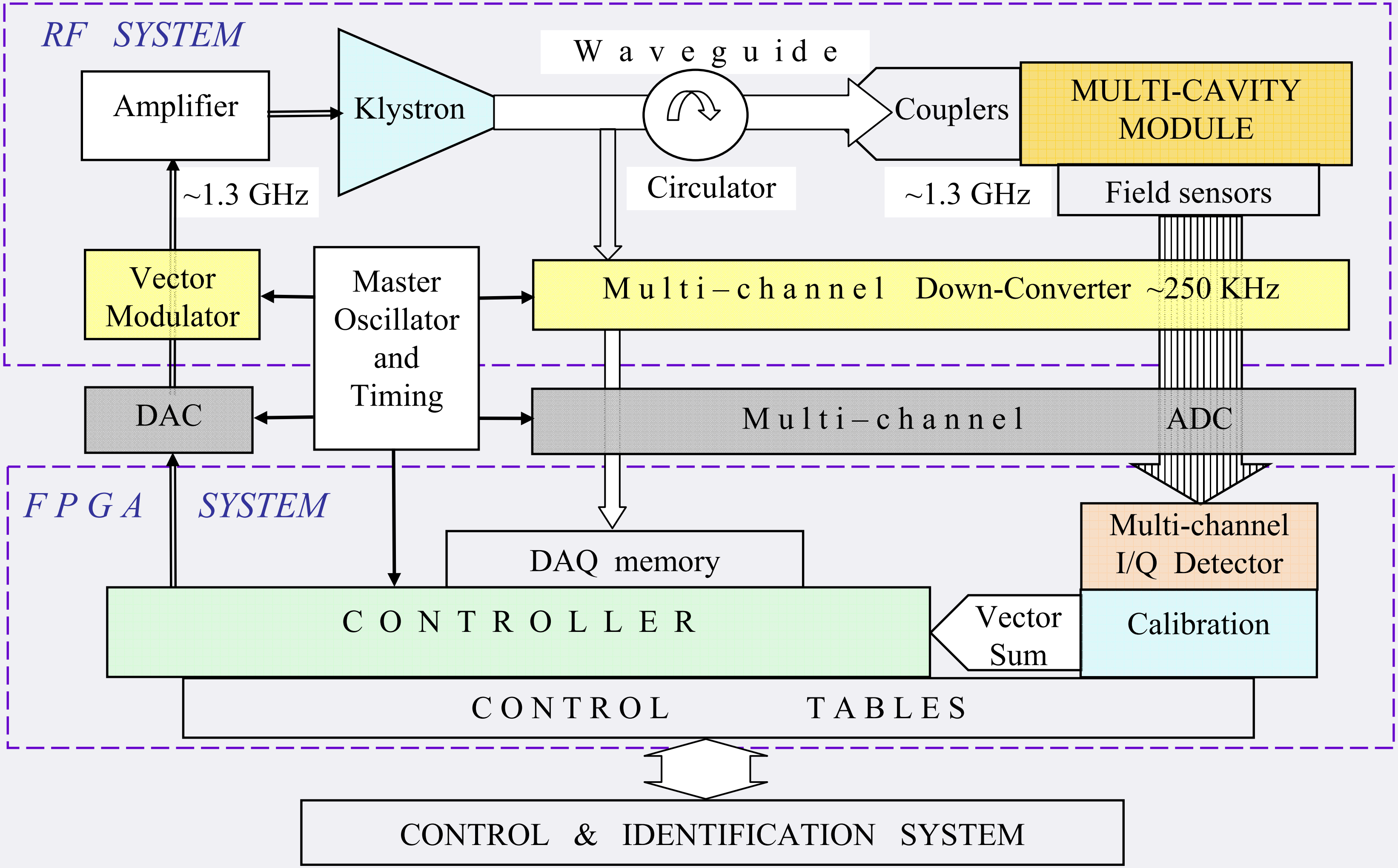


Low Level Applications

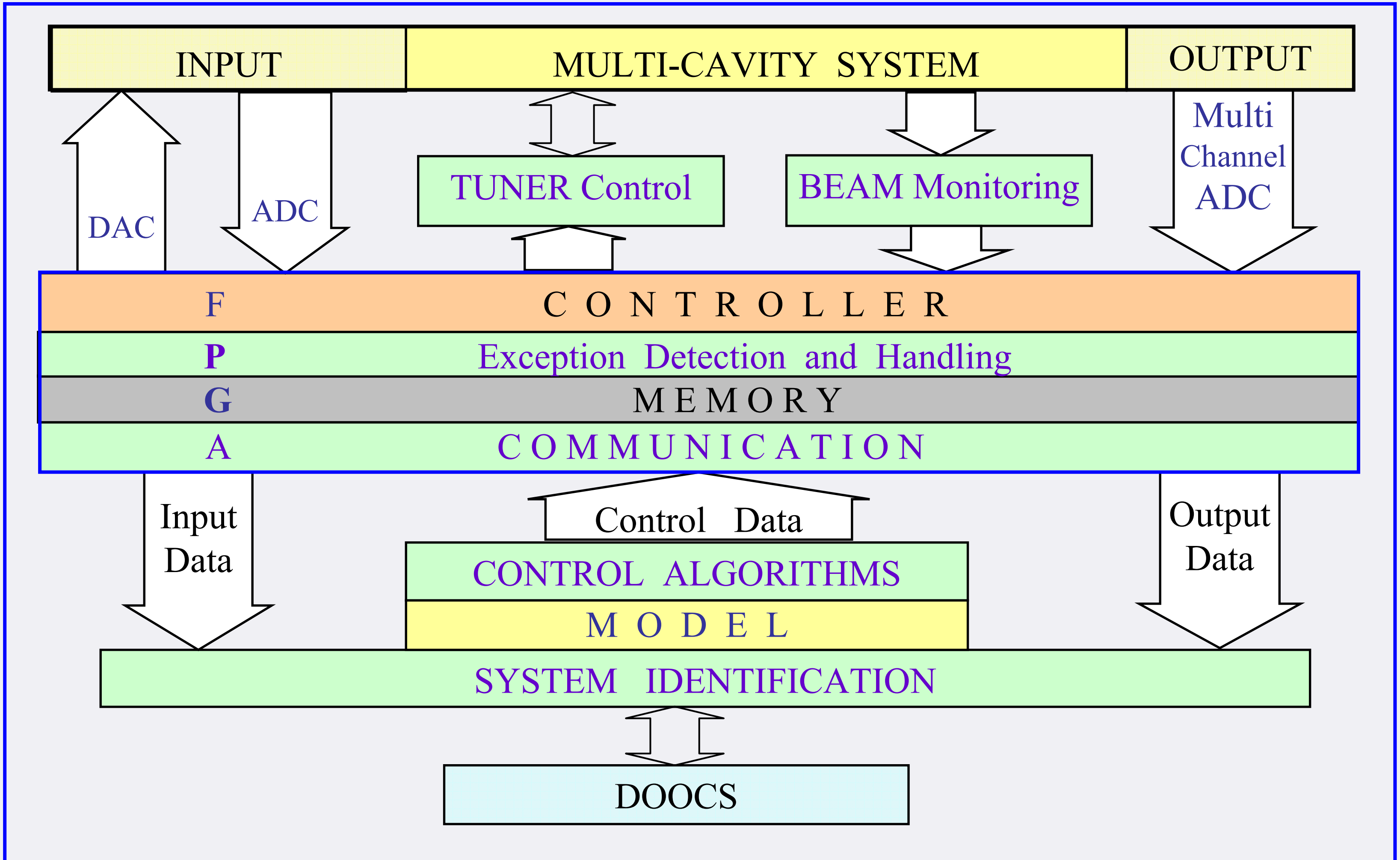
Procedures and supplementary data processing necessary to execute control algorithms

1. Communication
2. System Identification
3. Control Algorithms
4. Beam Monitoring
5. Tuner Control
6. Exception Detection and Handling

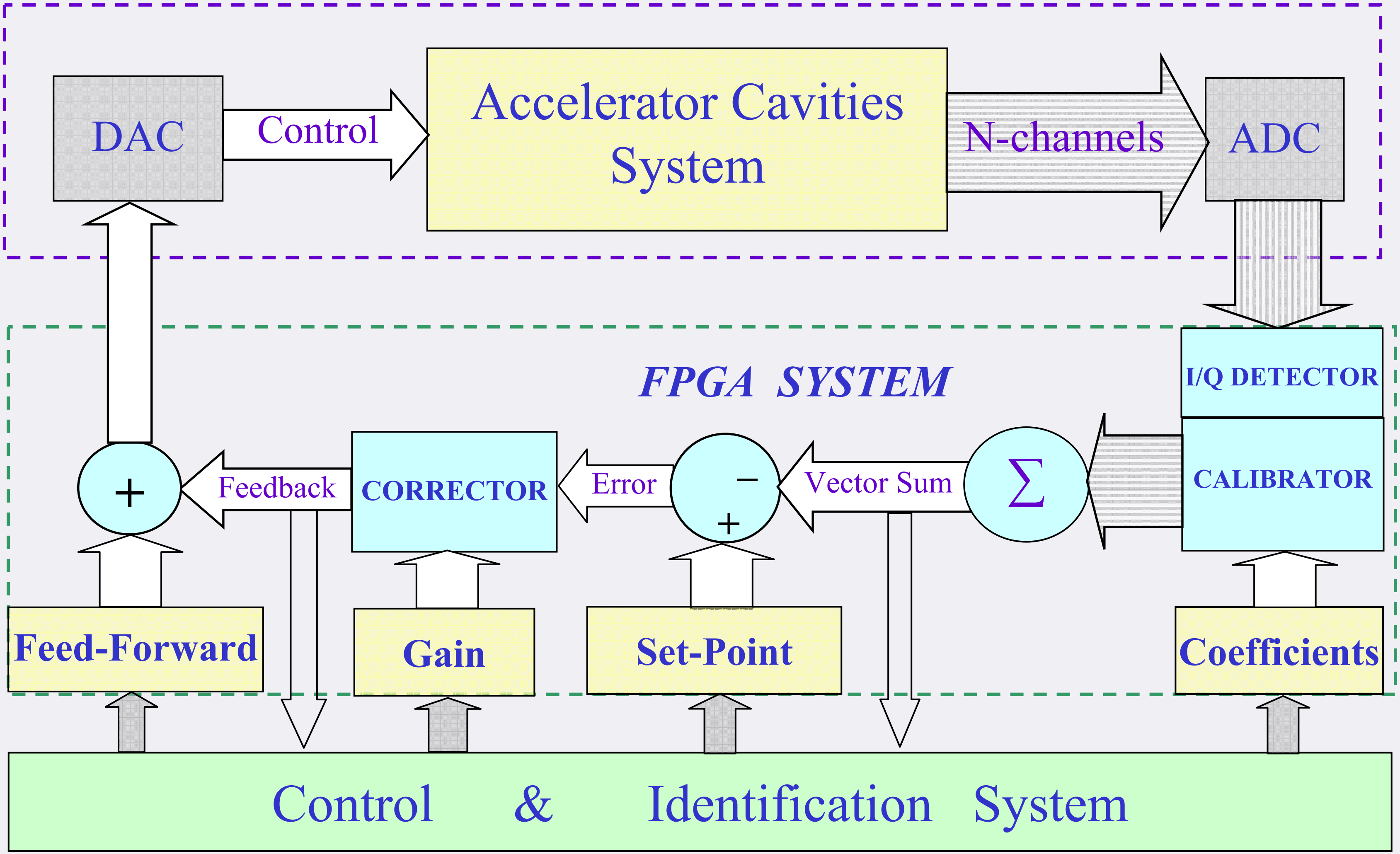
Functional block diagram of LLRF control structure



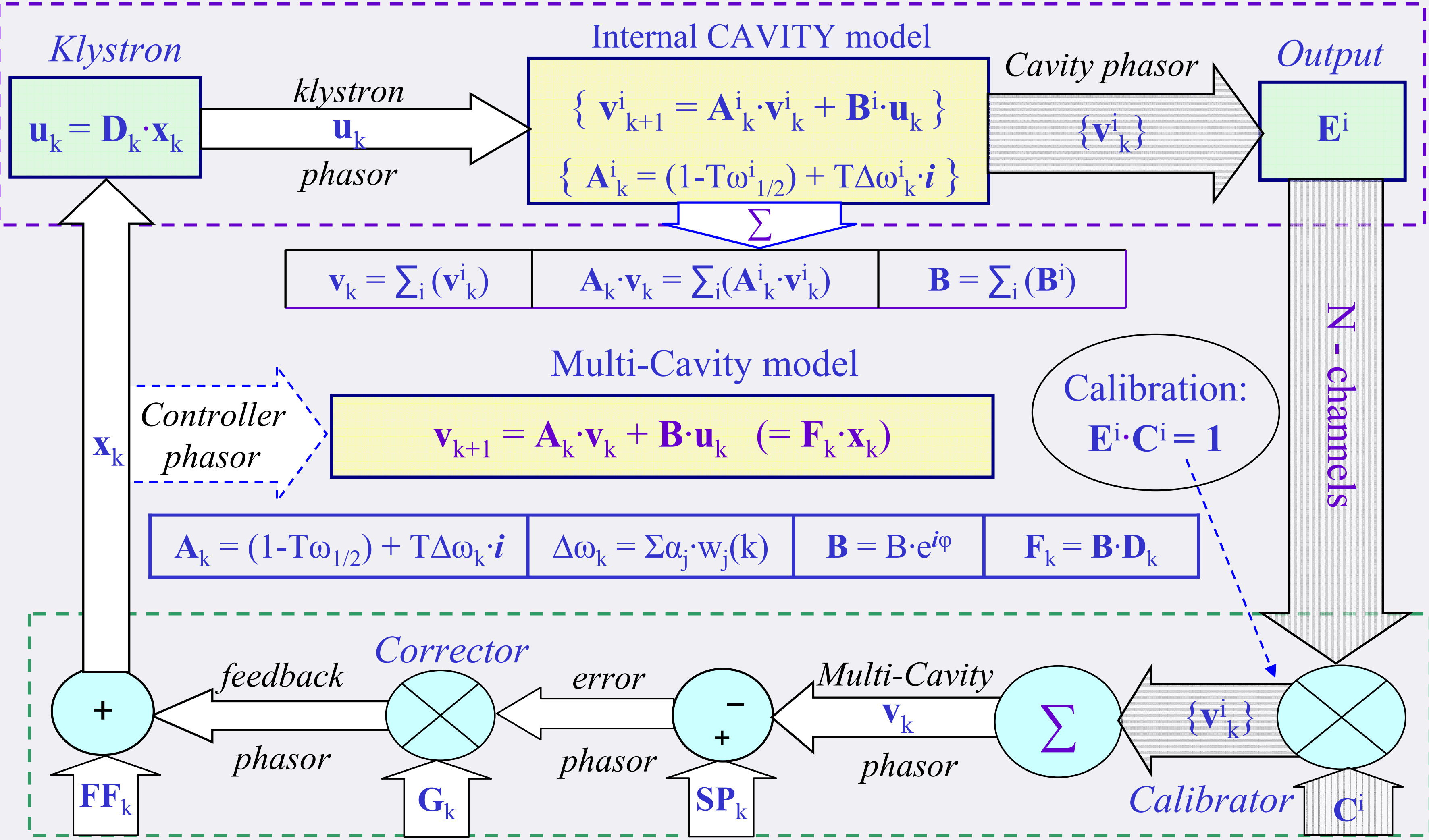
Low Level Applications functional arrangement



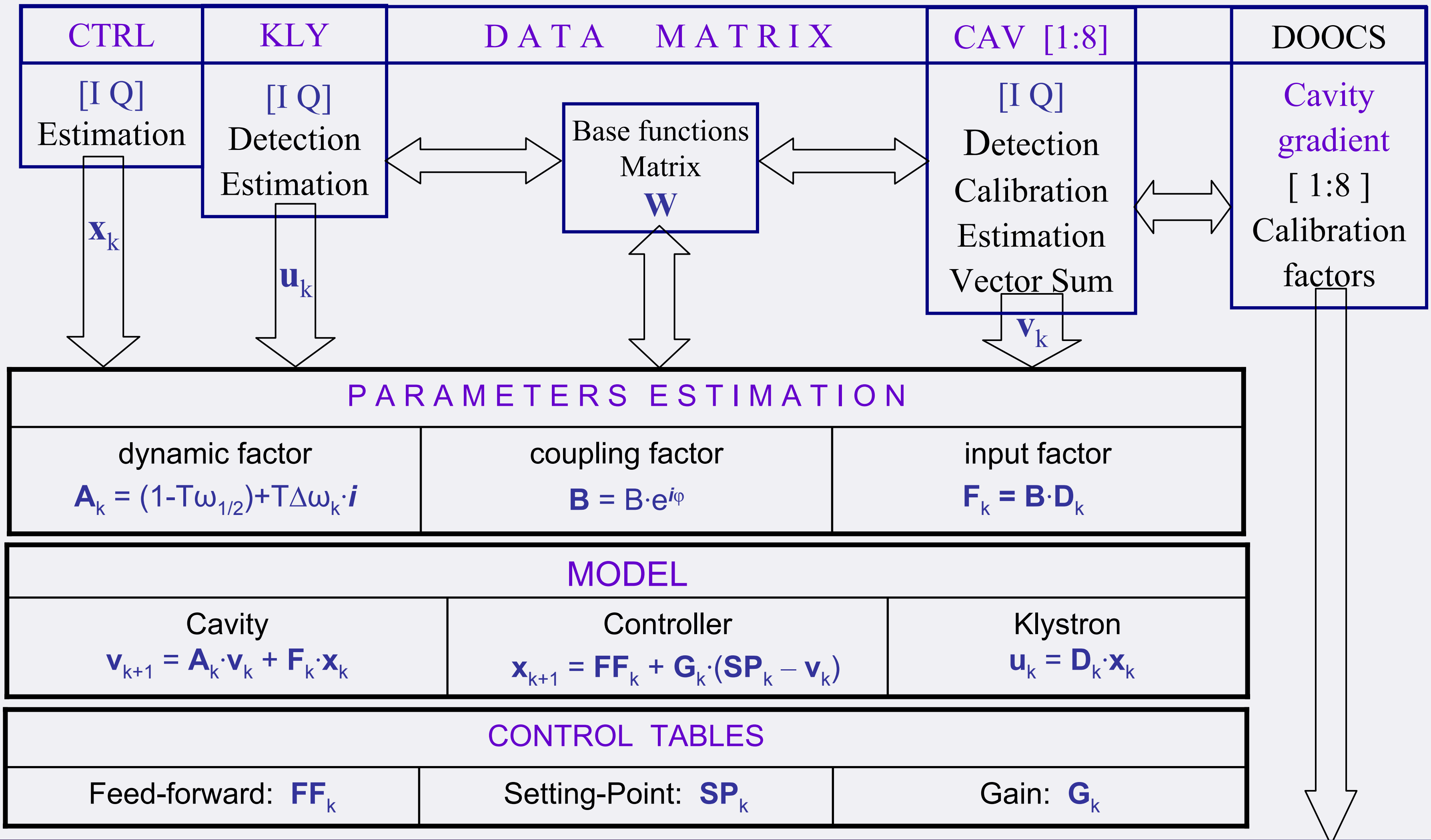
Functional block diagram of Multi-Cavity Control System



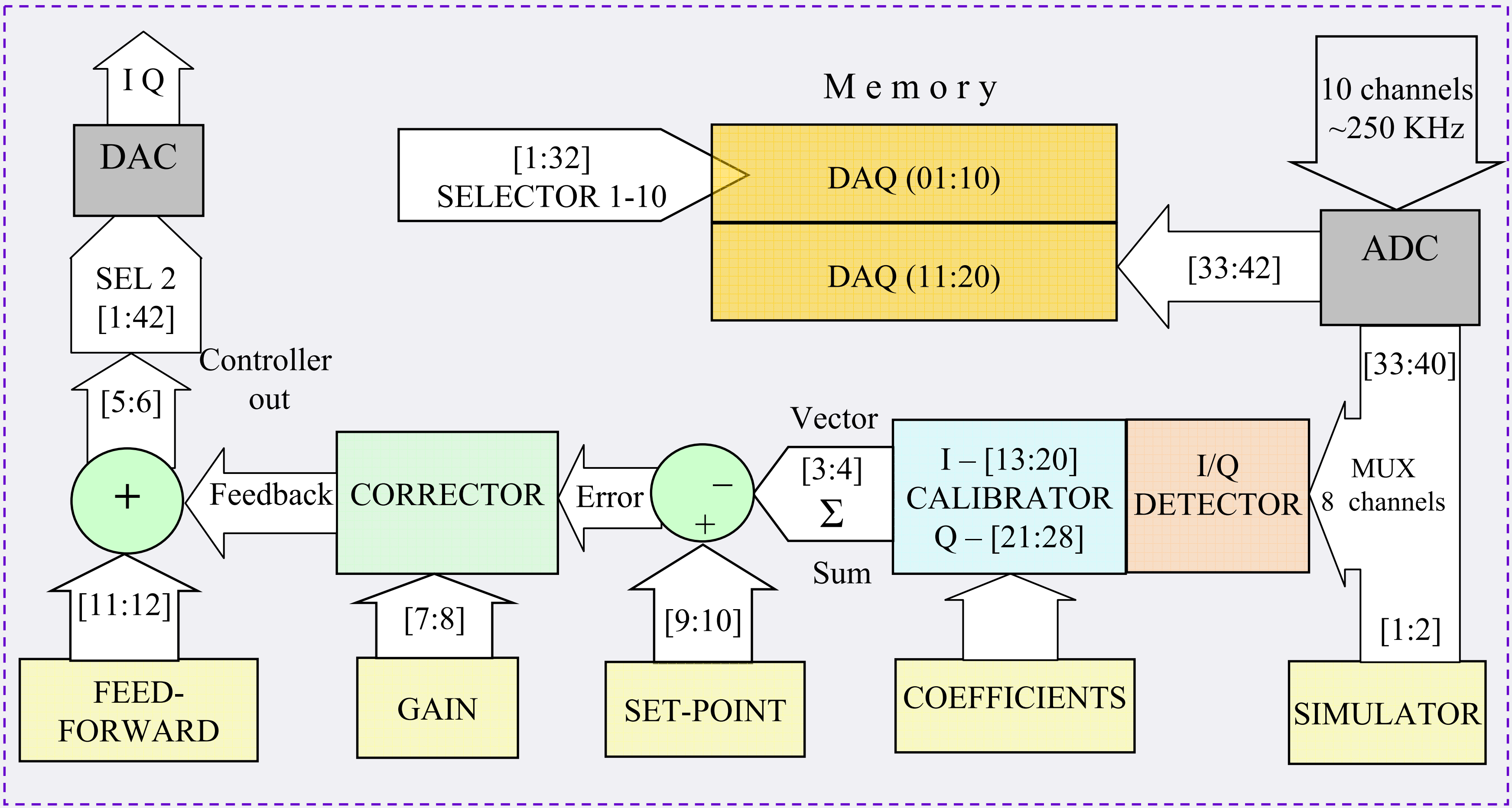
Algebraic model of multi-cavity control system



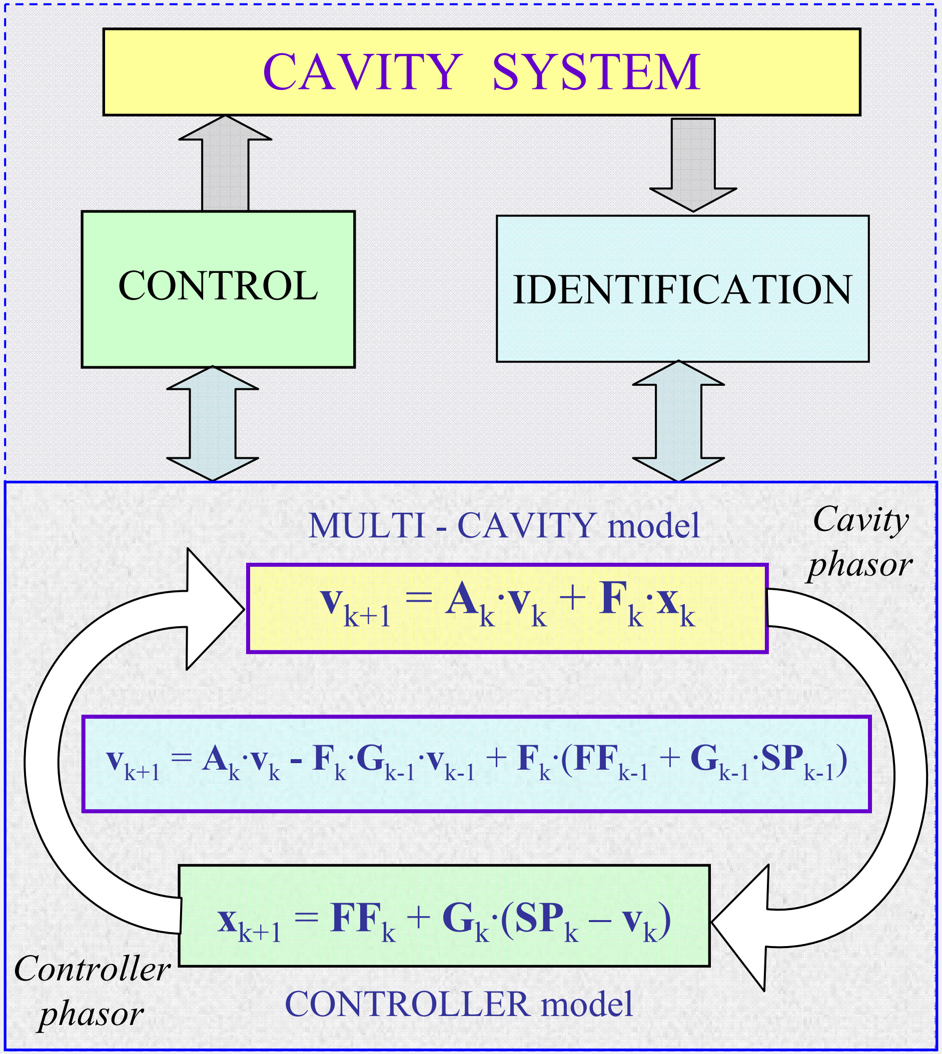
Cavity control system
Functional block diagram of MATLAB implementation

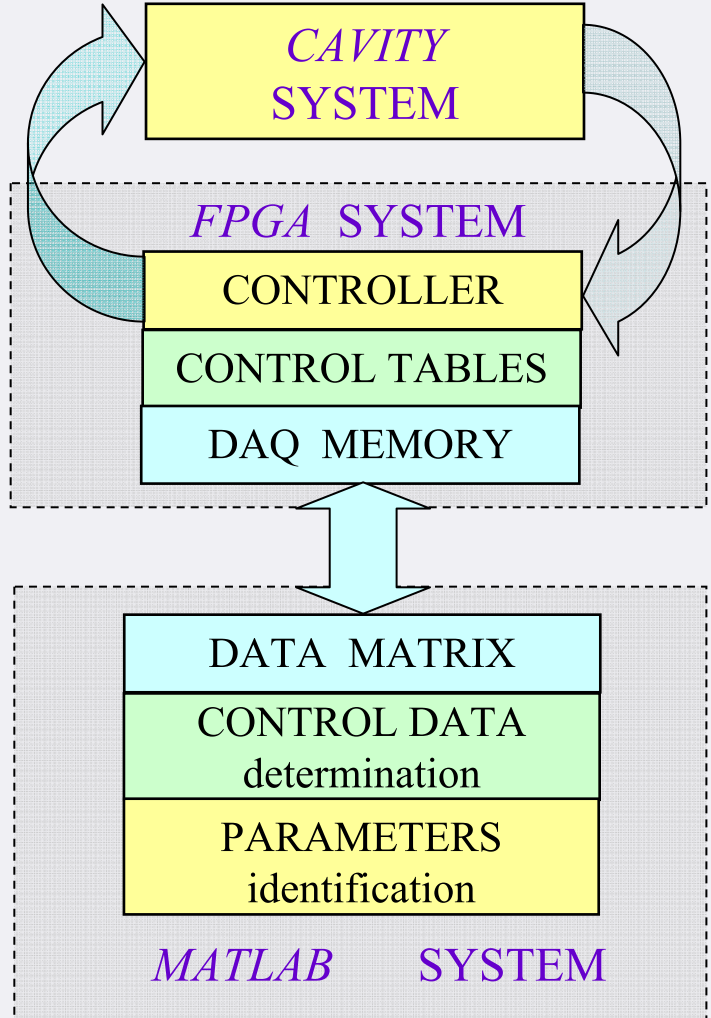


The functional block diagram of the FPGA controller structure with channel numbers of data flow

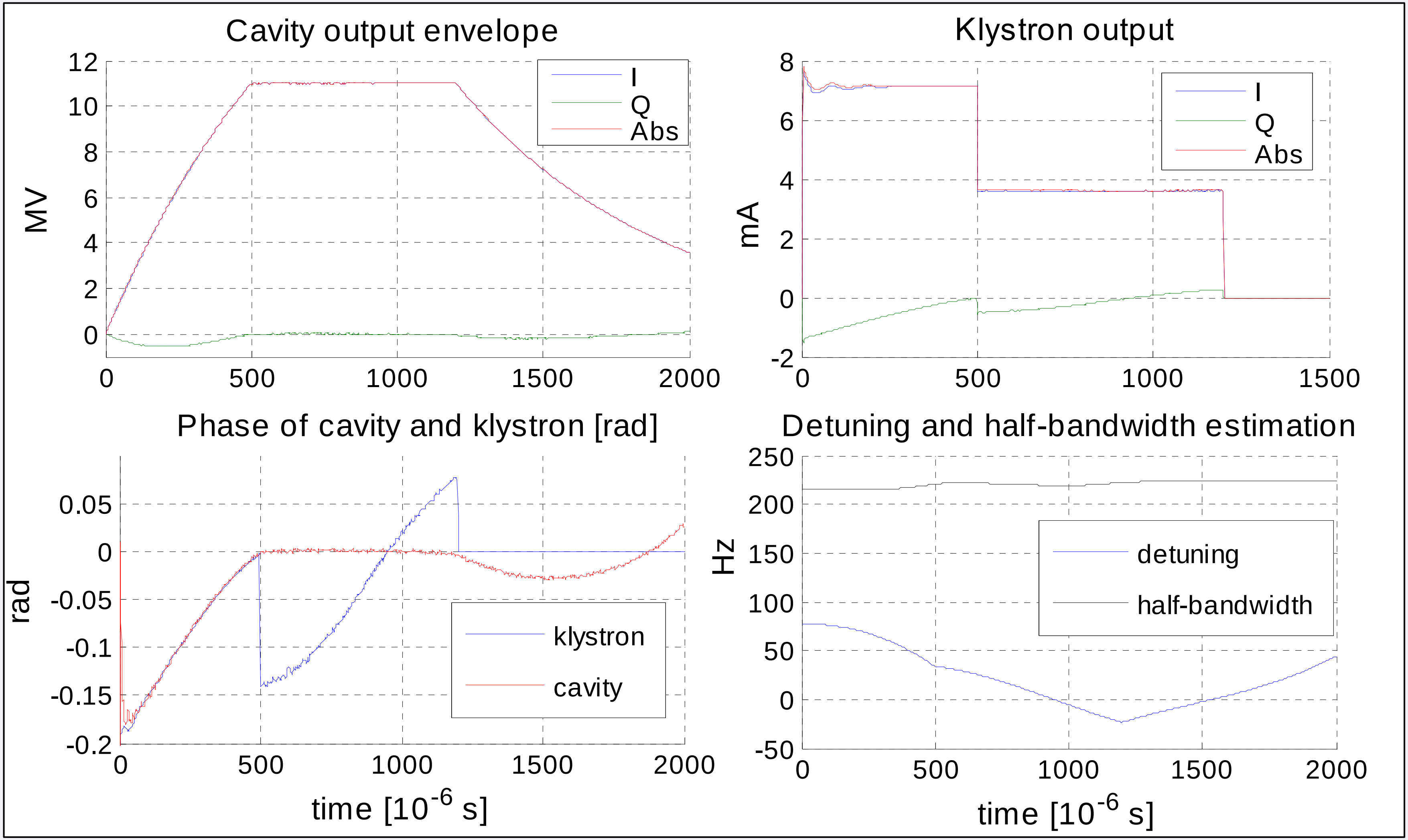


Adaptive Control Algorithm based on System Identification

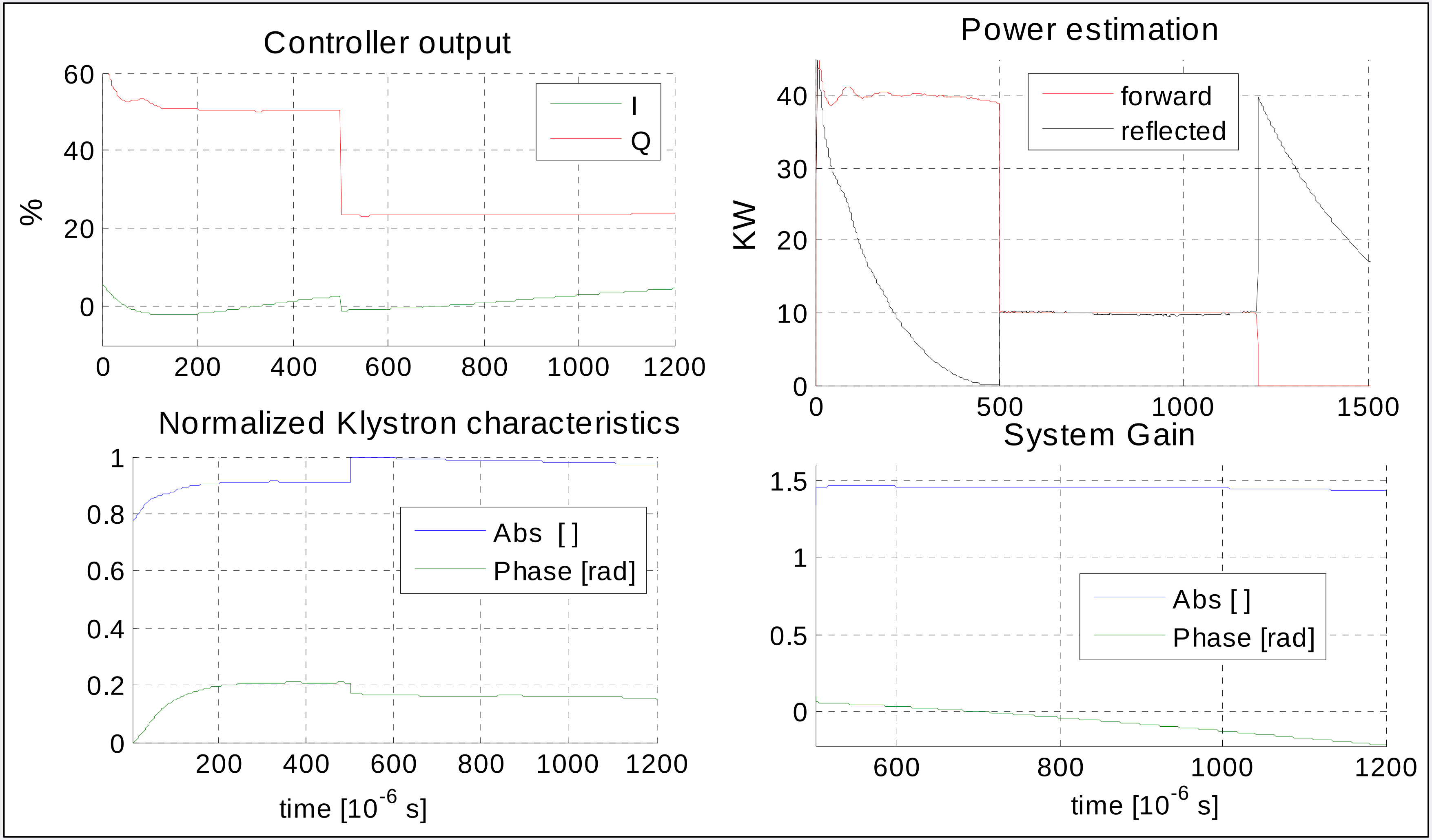




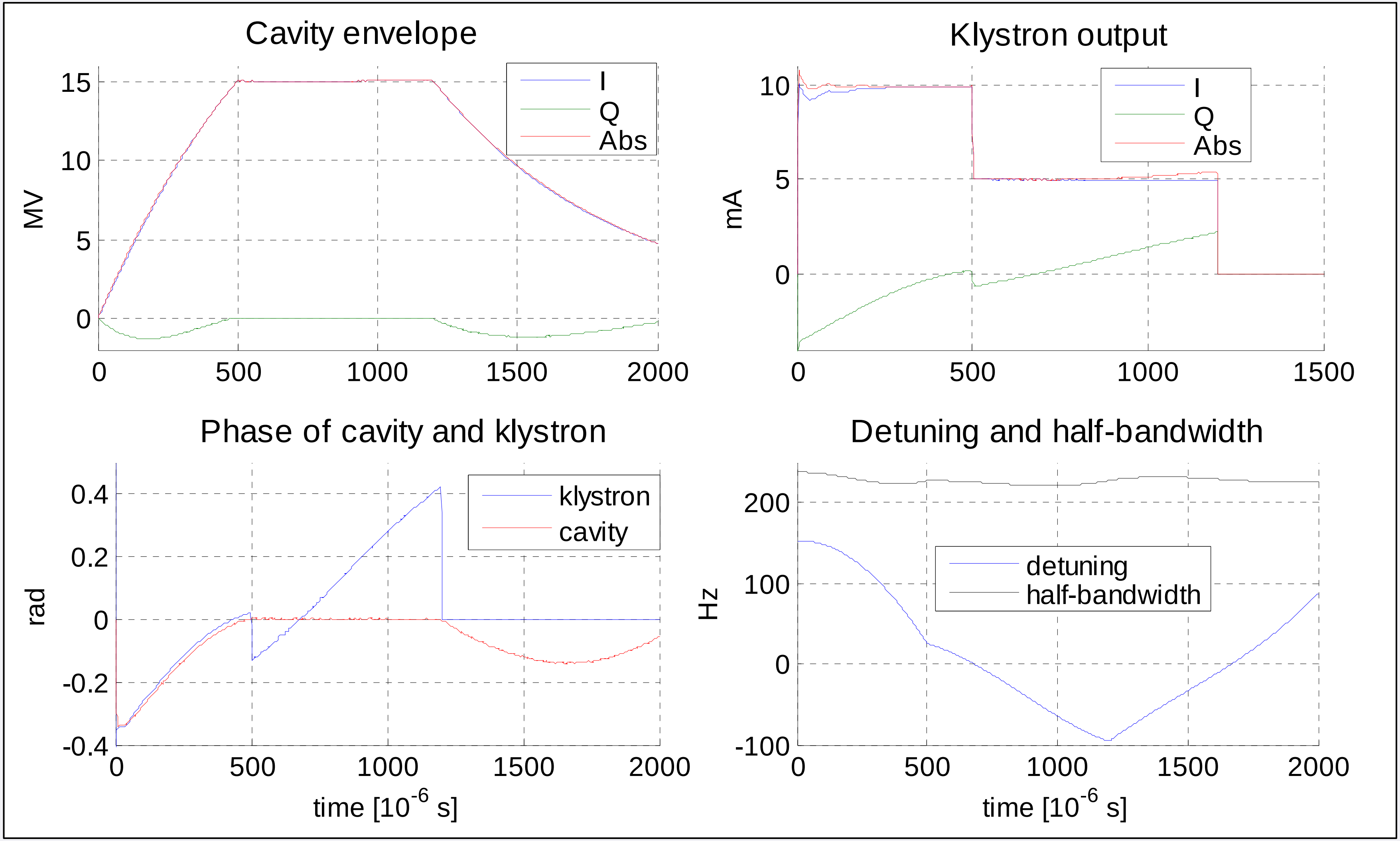
Single cavity control (ACC1 – cavity 4) Adaptive Feed Forward (gain = 0)



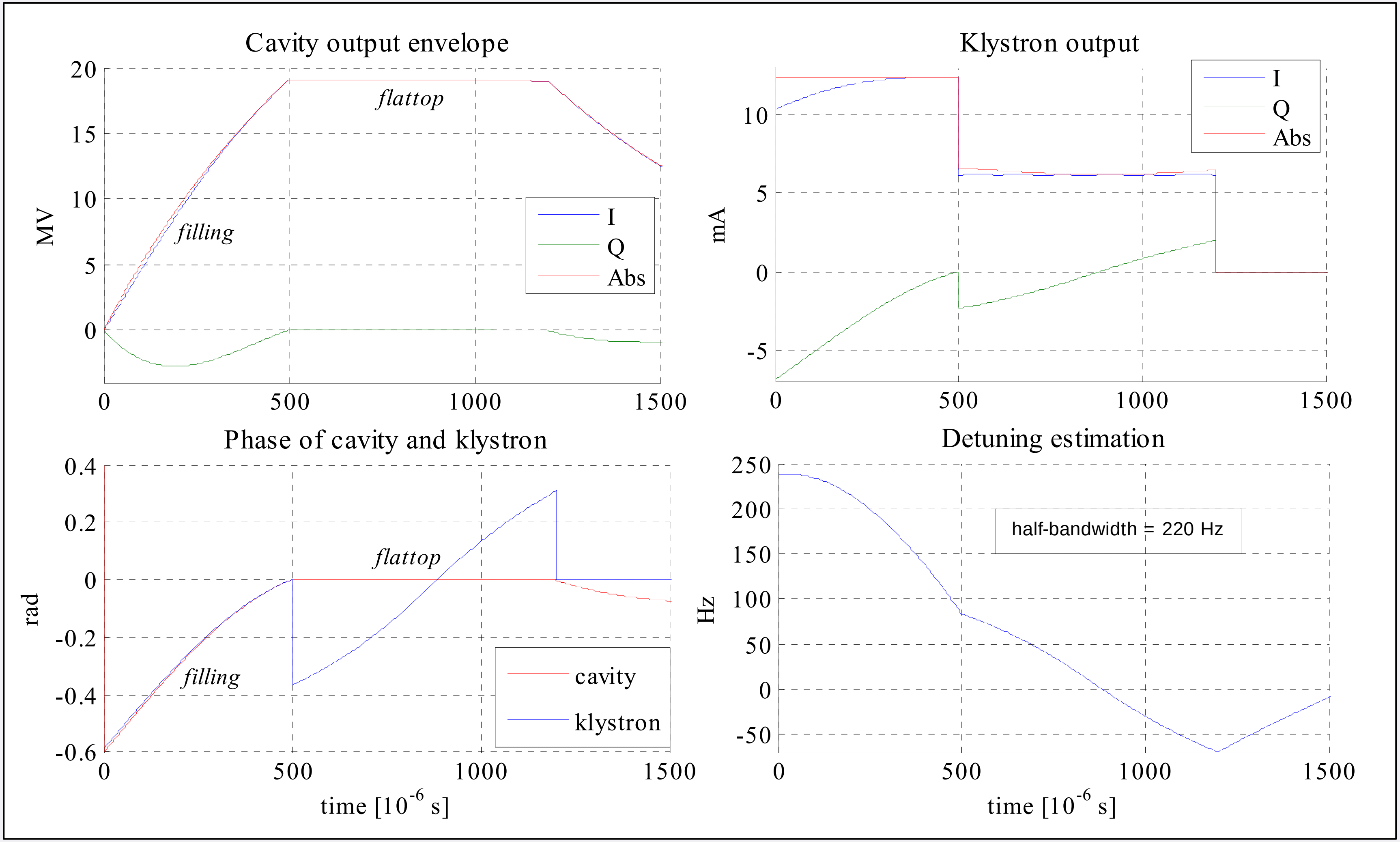
Single cavity control (ACC1)
Adaptive Feed Forward (gain = 0)



Vector sum control of 8 cavities – ACC1
Adaptive Feed Forward (gain=0)



Vector sum control of MTS module
Adaptive Feed Forward (gain=0)



Thank you for your attention