ATCA Based Controller

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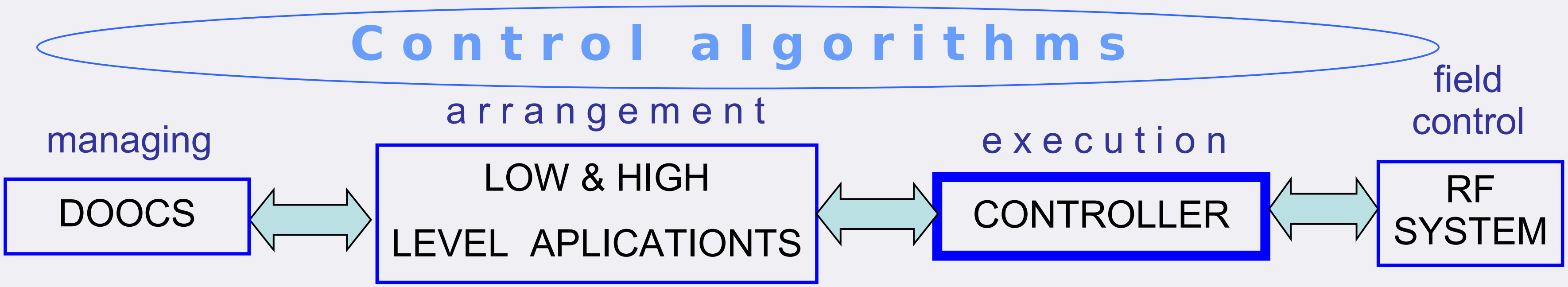
Controller definition

Simple & low latency automat stabilizing the amplitude & phase of electrical field during the single pulse



TASKS:

- **Execution of control algorithm basing on Control Data provided by Low Level Applications and on results of measurement of the Input signals.**
- **Providing of processed measurement data to the Low Level Applications layer**
- **Monitoring and Exception Handling for safety requirements**

Requirements for the controller

- Basic technical requirements
  - Multiple input channels
  - Low latency (as low latency as possible, however it depends on IF and technological limits)
- Modular, parametrized and reconfigurable structure
  - Modularity - It should be possible to distribute the design between a few AMC boards, and even between a few ATCA carrier boards (however it will impose some additional latency)
  - Parametrized – the number of memory blocks, of DSPs used, of input channels serviced may be changed without significant redesign
  - Reconfigurable – the general structure of the controller will be stable, even if some blocks are moved from FPGA to DSP.
- Design methodology related requirements
  - Controller is supposed to be a complex system, to assure high maintainability e.g. to avoid human errors the automatic implementation methods (DSP on FPGA, DOOCS integration) must be developed
  - Full testability is needed (in simulation, with real hardware, with hardware-software cosimulation)

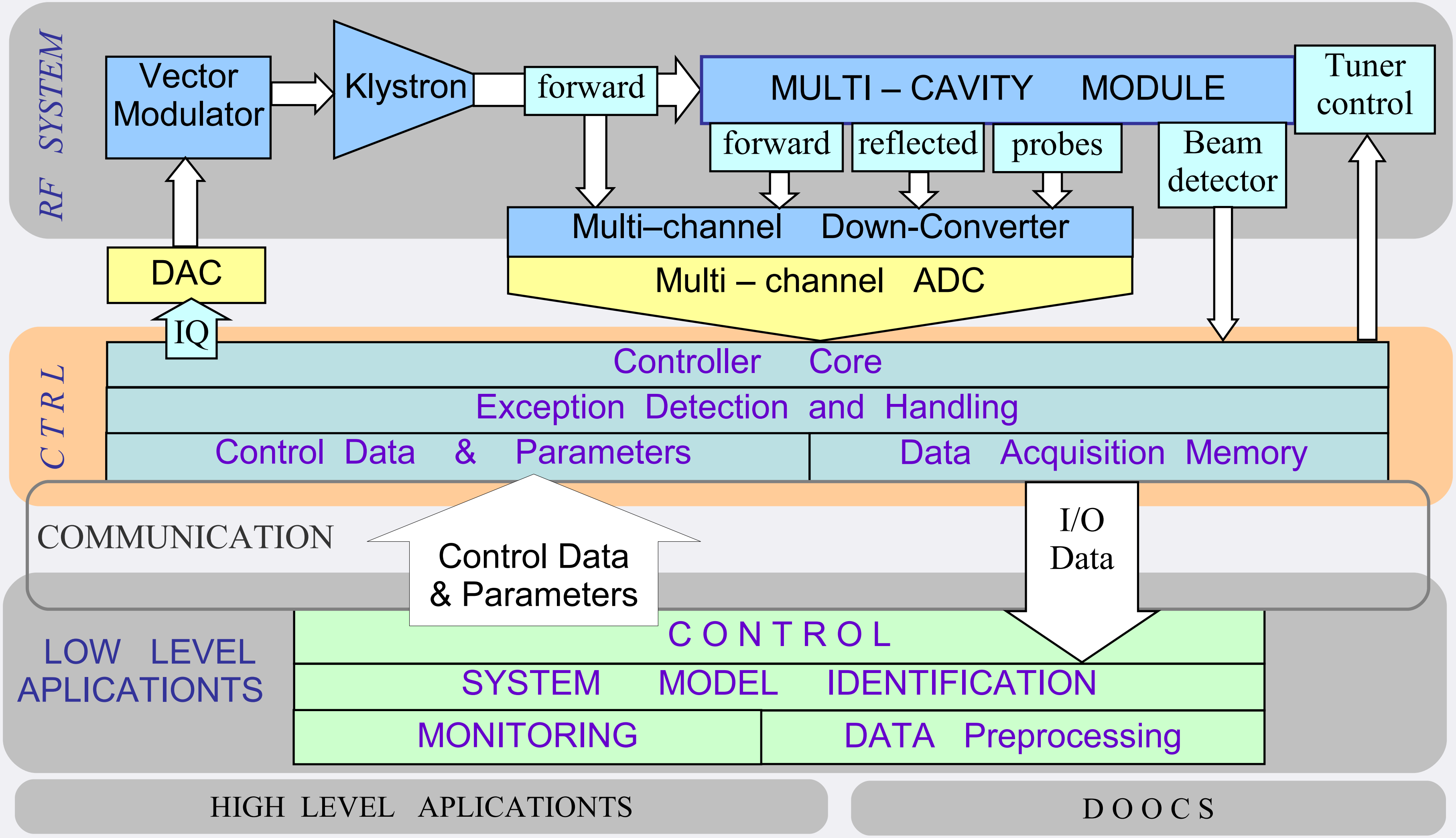
Reliability requirements of the XFEL controller

- Required: Continuous operation, one maintenance day per month
- ATCA provided functions for increased availability:
  - Redundant power supply
  - Full mesh topology – no global bus for boards' interconnection, which could be blocked by a damaged board
- Controller design features contributing to increased availability
  - Algorithm able to operate even when some analog inputs are failed
    - Use of redundancy in the analog input signals
    - Possibility to work with limited number of signals
    - Use of feed-forward alone as the „last resort solution"
  - Possible redundant implementation of the controller
  - Exception handling (e.g. Cavity gradient monitoring)

Functional requirements for the controller

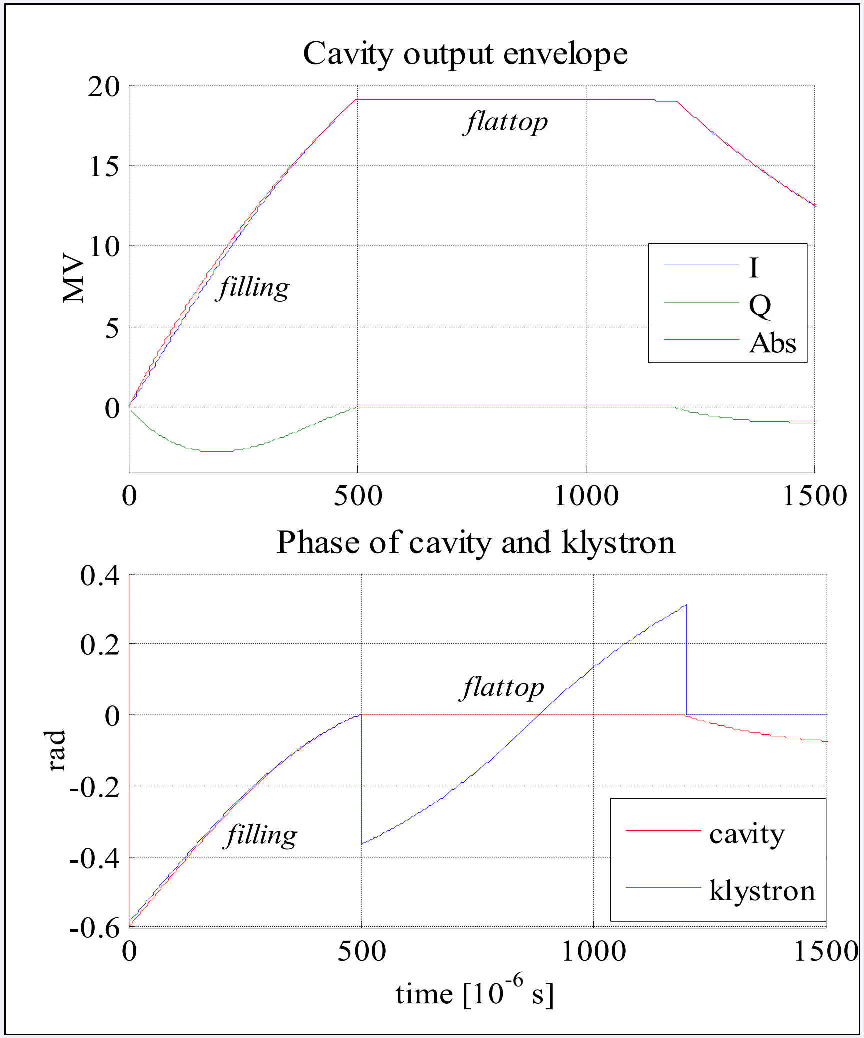
- Channel calibration
- Vector sum
- Error calculation
- Feed forward
- Generation of output signals with klystron linearization
- Provision of measured data for:
  - Low Level Applications layer for updating of Control Data for the Controller
  - For monitoring (DOOCS) and diagnostics (Exception Handling)

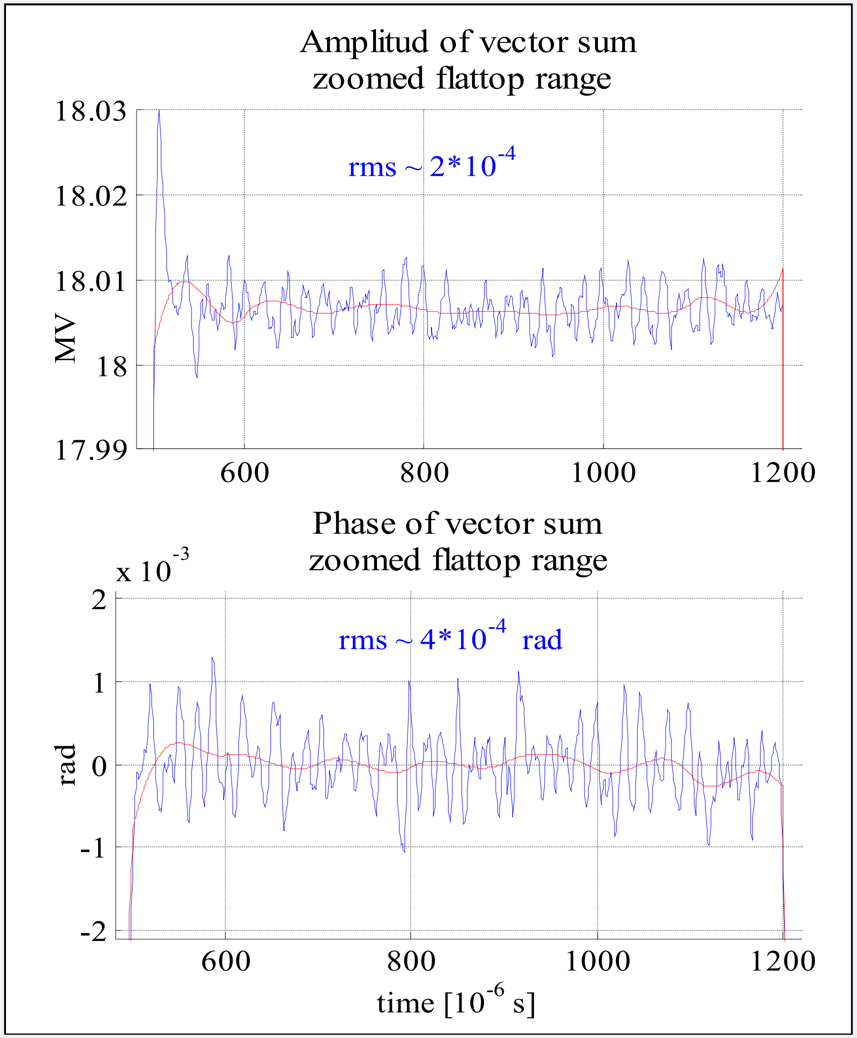
Outline of the LLRF control structure



Vector sum control – results from MTS tests

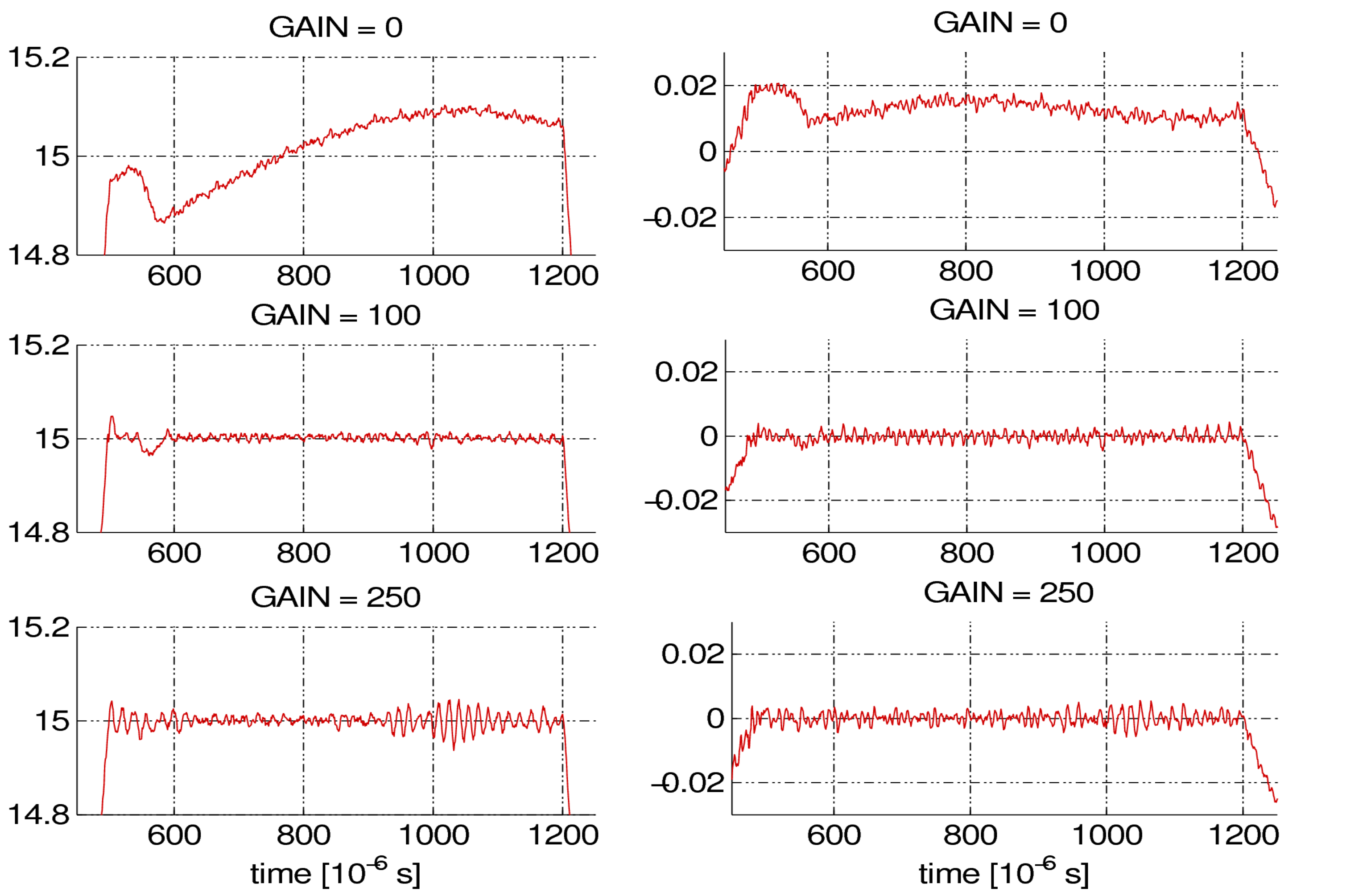
Adaptive Feed-Forward (gain=0) Feed-Forward + Feedback (gain=100)





Vector sum control – with beam, without FF compensation

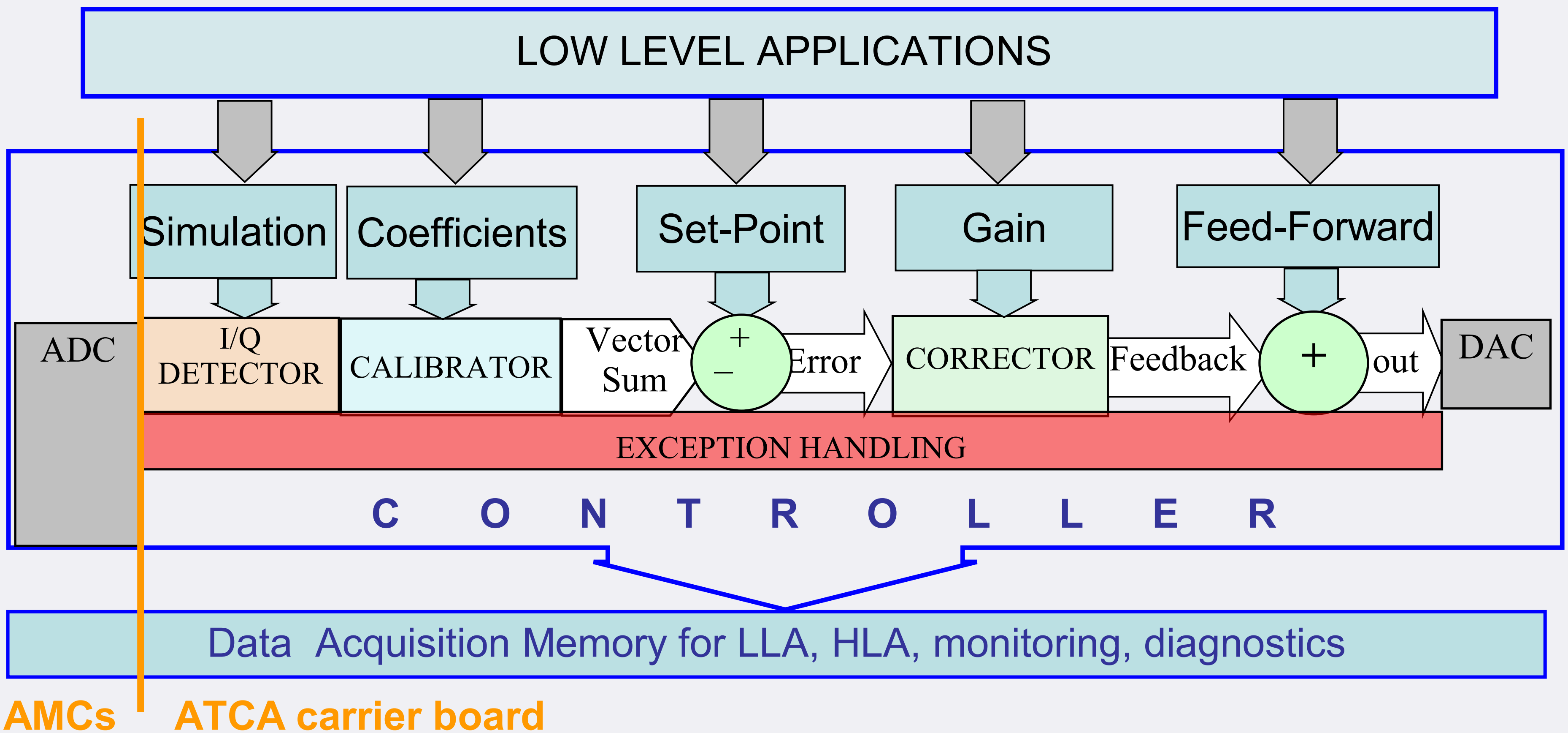
CAVITY FIELD AMPLITUDE [MV] CAVITY FIELD PHASE [rad]



Multiboard implementation of the controller

- Single board implementation impossible:
  - Main problem – multiple A/D converters (96 channels needed)
  - reasonable limit: 8 or 12 channels/board
- It is necessary to transmit the converted signals between the boards
- If possible, it will be preferable to split the algorithm between the boards

Functional Concept of Controller



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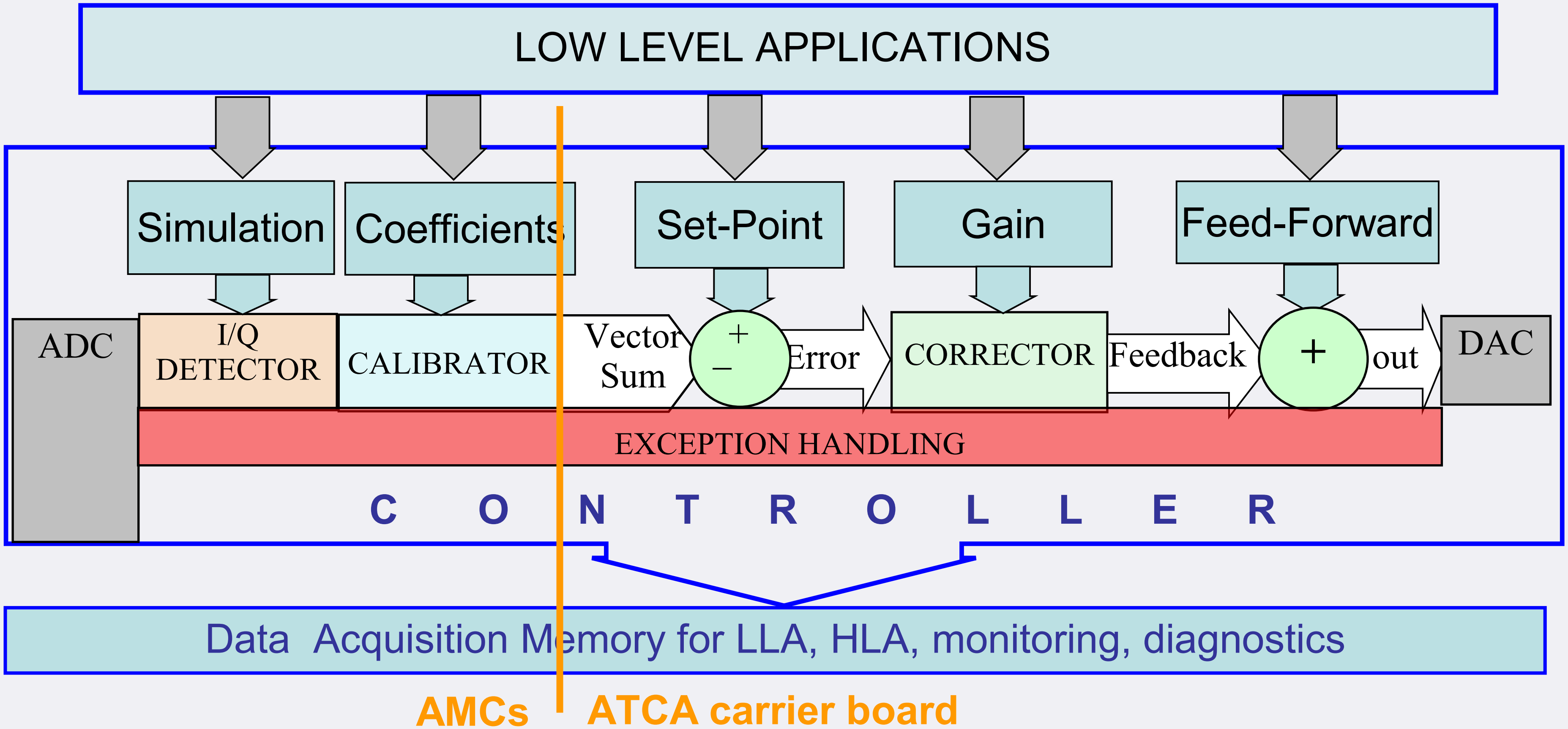
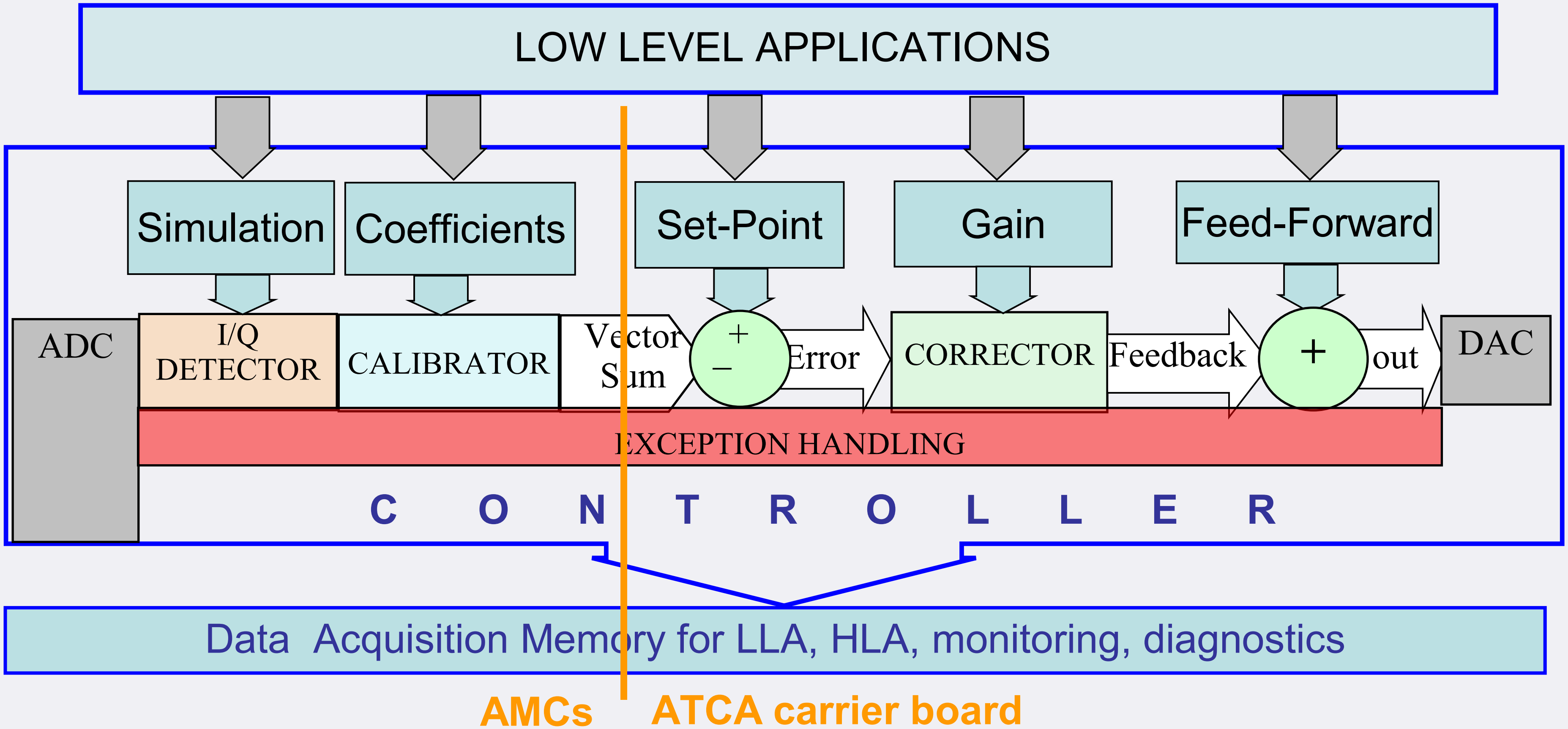
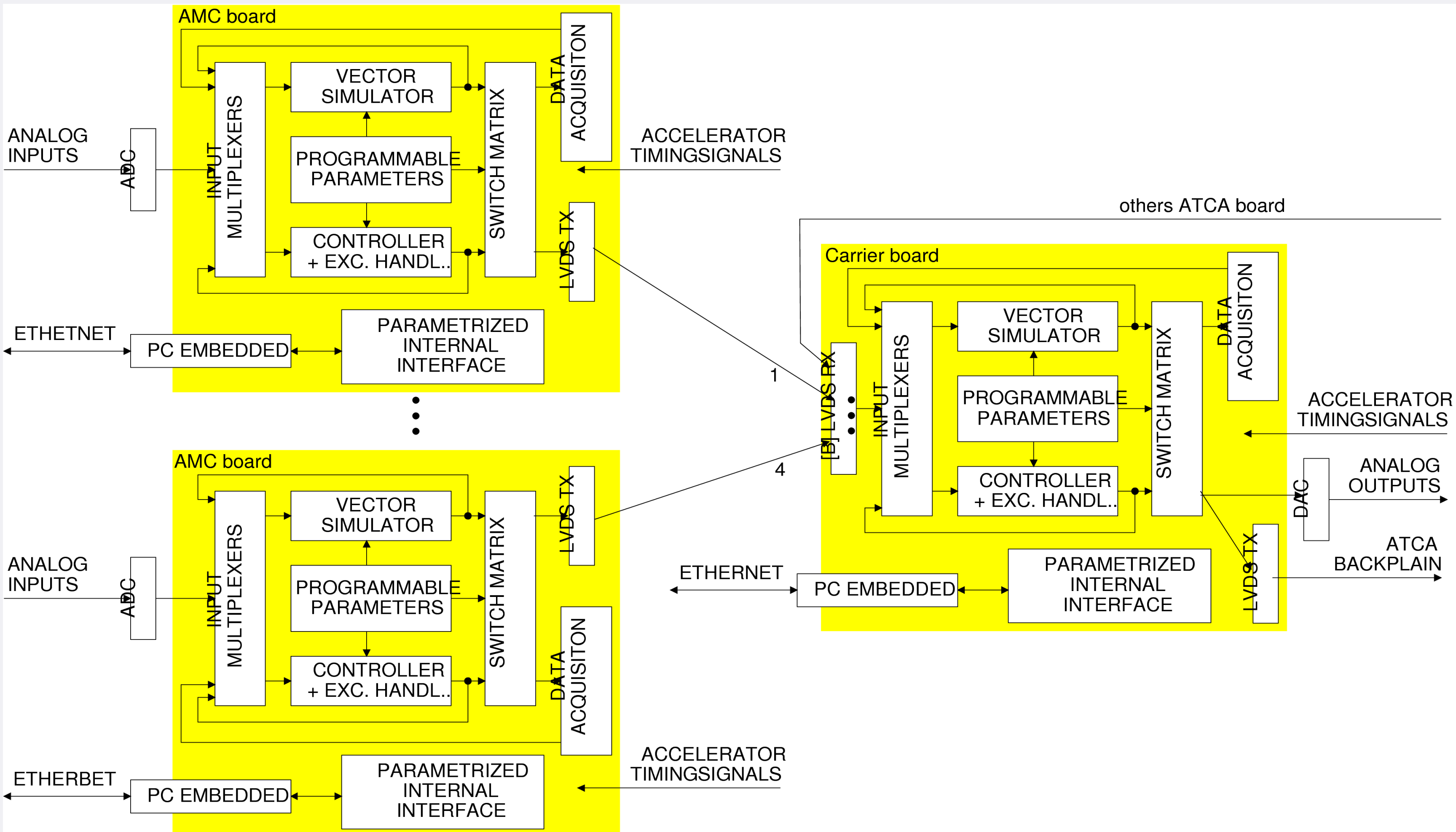


Functional Concept of Controller



Structure of the ATCA LLRF controler



ATCA communication capabilities used in the distributed controller implementation

- Low latency LVDS links provided by ATCA are essential for fast exchange of information between the distributed components of the controller

- Ethernet interface supports communication with the DOOCS system

Scalability of the XFEL controller

- The controller algorithm may be distributed between the FPGA chips, DSP processor(s) and general purpose CPU
- The number of ATCA carrier boards used to implement the controller may vary (depending mainly on the amount of inputs)
- The ATCA architecture allows us to use multiple AMC modules, multiple exchangeable AMC modules may be used
  - DSP modules
  - FPGA modules
- Fast communication interfaces allowing data exchange between the AMC modules may be used to efficiently implement distributed algorithms
- Number of installed modules may be suited to the needs of the algorithm

Debugging of the XFEL controller in the ATCA architecture

- Debugging and continuous monitoring of integrity of procesing is essential for such distributed system
- Efficient debugging of the firmware requires fast communication links to transfer the debugging and control data
- The ATCA architecture provides the following features usable for that purpose:
  - Ethernet link to each carrier board
  - PCI Express link to each AMC board
  - JTAG connection to each AMC on the carrier
  - LVDS interfaces to AMC boards (may be used for custom debugging interfaces)
- IPMI Interface („last resort solution” - low speed)

Development activity proposal

Development team

- ISE Employees
  - Wojciech Zabolotny, PhD
  - Krzysztof Pozniak, PhD
  - Tomasz Czarski, MSc
  - Maciej Linczuk, PhD
- IPJ Employees
  - Jaroslaw Szewinski, MSc
  - Grzegorz Plebański, MSc
  - Krzysztof Sajna, Msc
- DESY Employees/ISE PhD stud.
  - Waldemar Koprek, MSc
  - Piotr Pucyk, MSc
- DCMS PhD Students
  - Wojciech Jałmużna, MSc

Tasks realization

- Controller
  - Controller Core
  - Exception Detection & Handling
  - Control Data & Parameters
  - Data Acquisition Memory
- Integration with „communication" package
- Simulation
  - Integration with LLA simulation

Schedule (heavily depends on hardware availability) – 24 m.

- Development on the existing SIMCON hardware (due to portable design) – 12 m.
- Tests in simulation – 15 m. (in the background)
- Porting to target platform – 12 m.

Conclusions

- The proposed implementation of the Controller has been successfully verified in the FLASH experiment
  - however further work is needed on: exception handling, monitoring and diagnostics, optimal distribution of algorithms (with LLA) between available resources, integration with the communication
- The Controller design is very tightly associated with the design of Low Level Applications and Communication
- Features of the ATCA technology useful for implementation of the LLRF controller
  - High reliability architecture
  - Scalability – both on the crate level and on the carrier board level
  - Low latency connections between carrier boards and between AMC boards
  - Big amount of backplane connectors available for the user and full mesh connections in the ZONE2 area for easy acquisition and concentration of multiple analog signals