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FPGA based, modular, configurable controller with fast synchronous optical network

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ABSTRACT

The paper describes a configurable controller equipped with programmable VLSI FPGA circuit, universal expansion modules PMC, synchronous, optical, multi-gigabit links, commonly used industrial and computer communication interfaces, Ethernet 100TB, system of automatic initialization ACE etc. There are characterized the basic functional characteristics of the device. The possibilities of its usage in various work modes were presented. Realization of particular blocks of the device were discussed. Resulting, during the realization of this project, new hardware layer solutions were also characterized.

Keywords: measurement-control systems, distributed systems, programmable circuits, FPGA, behavioral programming with parameterization, VHDL, optical multi-gigabit transmission, industrial communications interfaces,

1. INTRODUCTION

As a result of abrupt technological development during the last two decades, the following current resources of the largest FPGA circuits by Xilinx [0] and Altera [2] are available in a single chip:

- several thousands of configurable logical blocks,
- ten megabytes of parameterized static memory,
- above one thousand of configurable user pins with the possibility to program a single pin in around twenty signal I/O electrical standards (and soon optical) like: asymmetric or symmetric, LVDS, TTL, PCI, CMOS, etc.,
- two hundred fast blocks of numerical processing like: fixed point multiplication circuits or multiplication-adding [3,4],
- around 20 nondependent modules for multi-gigabit synchronous transmission links – electrical or optical [5,6],
- several embedded processors (Power-PC 407 [7] class in VirtexIIPro and Virtex4 by Xilinx [0]) or synthesized processors („NIOS" [8] type in FPGA circuits by Altera or „MicroBlaze" [9] type in FPGA circuits by Xilinx).

The above listed logical resources provide hardware environment for implementation of fast, multithreaded, and very complex functionally processes of feedback control, data registration, numerical processing, data analysis in the real time. The implemented standards of fast data communications like: Ethernet, Fast Ethernet, RocketIO [10], PCI, LVDS, enable realization of modular complex distributed systems (network like) of: data transfer and acquisition, control, monitoring, diagnostics, standardized communication channels with supervisory computer systems.

Application of large FPGA circuits, with large configurable resources and rich peripheries, for realization of configurable controller gave a solution which is stable structurally, programmable functionally, concentrates a large number of functions, is highly integrated, and has a very large developmental perspective. The controller was assumed to occupy a single PCB with the possibility of expansions via small daughterboards. The latter realized in PMC mechanical standard. The controller may be configured as a standalone device, several devices clustered in a single hub in standard industrial crates, or several devices networked via optical links. Practical availability and application of a universal controller enabled the system designers to realize a variety of measurement-control systems and networks. Standardization of the hardware layer, software layer and a lot of close integration between them, considerably decreases the system realization costs, and realization time of the whole practical system.

2. FUNCTIONAL STRUCTURE OF CONTROLLER

The controller was designed in the form of a base PCB, in mechanical standard EURO-6HE-160 fitted to industrial crates with VME/VXI interfaces [11, 12]. Fig. 1 presents a general functional diagram of the controller.

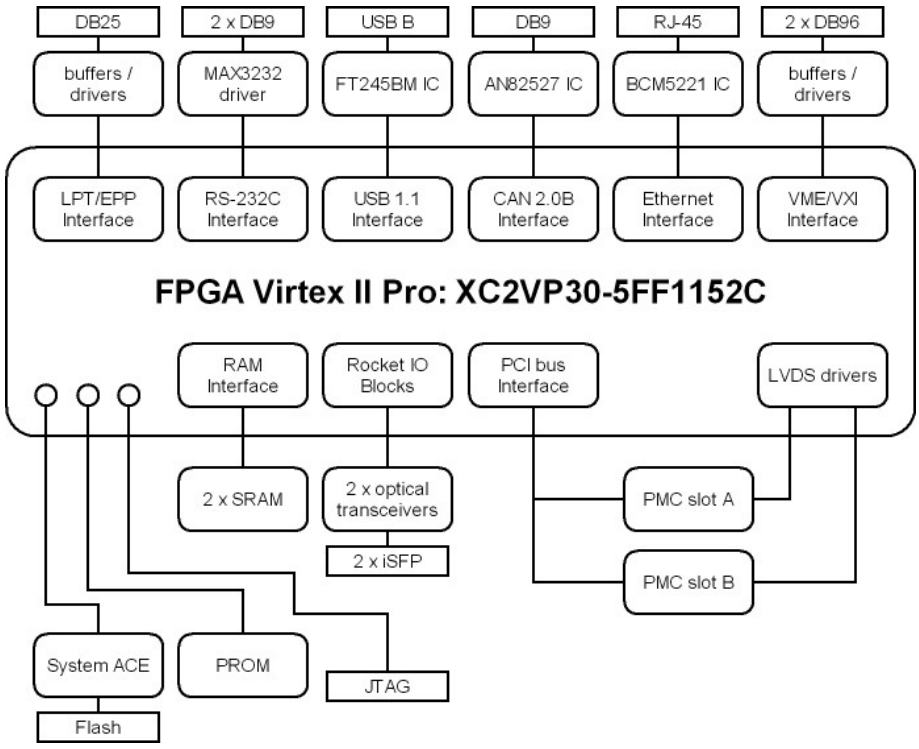

Fig. 1 Basic functional blocks of controller

A programmable circuit FPGA VirtexIIPro XC2VP30 [13] was used for realization of the integrated control module. This chip is a representative of the new generation circuits with the following resources:

- 30816 logical blocks (LCELL), where each block may realize independently, arbitrarily programmed , four-input, logical function,
- 136 embedded multiplication circuits 18x18 bits, realizing a single operation in 6-8ns time. Fast multiplication circuits enable FPGA based implementation of complex DSP algorithms working in the real-time,
- 2448 kB of memory with double access ports (DUAL-PORT SRAM). The memory is divided to 138 independently configurable blocks, each of 18kB capacity,
- 8 modules of distribution of fast clock signals (Digital Clock manager – DCM), which enable rescaling of the base frequency and keeping precise phase of clock signals,
- 8 modules of RocketIO input-output channels, which realize serial gigabit transmission. Each module may reach the maximum data transmission of up to 3.125Gb/s. The circuit solution enables for direct integration of RocketIO modules with optoelectronic transceivers [10]. There were applied commonly used optical fiber connectors of ST type.
- 2 embedded Power PC 405, RISC class microprocessors (CPU). The mathematical calculation unit of the μP includes hardware mathematical units and provides defining of special instructions by user [7]. The processors may work with distribution of LINUX operational system, real-time operational systems, or other.
- 644 outputs defined by the user to connect external electrical signals. Far particular pins, in a programmable way, there are defined electrical parameters like the choice of standard (TTL, LVDS, PCI etc.) or the direction of signal distribution (In/Out).

Application of a sufficiently large FPGA circuit enabled to concentrate all necessary functionalities of the designed controller in a single programmable chip. The rest of the devices positioned on the PCB are functionally the necessary peripheries.

The needed system peripheries provide to the controller, working as a measurement network node, needed booting initialization and configuration of the FPGA chip. Depending on the method of the controller PCB usage, the user may define a system initialization method, choosing one of the following three possibilities:

- programmable chip of EPROM type, which has a stable configuration program for Xilinx circuit [14]. EPROM content may be modified through new data transfer via JTAG interface. This solution was prepared primarily for the final user, which in practice does not modify alone the content of the FPGA configuration program itself. Rare and exceptional modifications of EPROM configurations are assumed. They result mainly from current service of the node or from the development of the node functionalities,
- system ACE, provides carrying out the booting processes of the controller from external FLASH disc embedded in the expansion memory slot [15]. Easy exchangeability of such a disc enables frequent and user friendly changes in the configuration of Xilinx circuit. This method of initialization was predicted for an user who may independently and frequently introduce the code changes for FPGA chip.
- JTAG socket, enables for direct connections between the programmable and monitoring circuit to FPGA [16, 17]. This is a solution dedicated to servicing and maintenance works, debugging, testing and commissioning. The content of FPGA configuration file is lost after switching off of the PCB power supply. The content has to be again transferred to FPGA by the programming device during the booting process of PCB.

The communication peripheral devices provide to the node direct contact with the external devices like: computers, other controllers, external measurement devices, etc. While realizing the interfaces, there were used the resources and properties of FPGA chip, and additional peripheral devices, buffers, voltage converters. The group of communication peripheries includes the following devices:

- Ethernet interface provides connection of the node with other computer devices via a standard, reliable and cheap network solution. Servicing of the signal layer is done by controller BCM5221KTP by BROADCOM, and the logical layer is serviced by a specialized functional block and Power PC microprocessor in Xilinx VirtexIIPro circuit. Ethernet provides compatibility for 10BaseT and 100BaseTX, and protects optimal management of power consumption, automatic control of cable lengths, and level of noise. It provides industrial standard for work temperatures and immunity to electrostatic discharges.
- CAN 2.0 interface enables direct connections of a node to a single CAN bus [18]. Provides transmission rate up to 1 Mbit/s for 1 km for a differential serial transmission. The interface services standard and extended data frames and remote callings. Provides global filtering masks and service for 15 objects for messages (14-two directional and a single transmitting) Has a mechanism of configurable interrupt vector. The interface assures transmission which fulfills the requirements for real-time systems. The CAN interface is predicted to configure the controller with auxiliary control-measurement devices, mainly commercial.
- USB interface provides serial transmission with the rate of 1 MB/s. Provides compatibility with standards usb1.1 and usb2.0. Possesses simple four signal handshake protocol, input and output FIFO buffers. Enables work mode in mass and isochronous regimes. Gives access to configurable parameters *VendorID*, *ProductID*, *SerialNumber*, *ProductDescription*. USB interface was implemented in order to connect easily the controller directly to a single user computer or a single peripheral device.
- VME/VXI interface, which enables for direct connections of the PCB to the most frequently used industrial standard buses VME-bus or VXI [11, 12]. Due to this reason, the mechanical construction of controller PCB was adapted to standard dimensions EURO-6HE-160 Euro crate, with VME-bus or VXI controllers. Hardware implementation of the VME-bus provides the node with the possibility to work in the following modes: SLAVE, MASTER and as a controller of the VME crate,
- Parallel interface EPP is characterized by simplicity in hardware realization and high popularity. It enables integration of the node with measurement apparatus and peripheral devices of older types and with cheap own solutions. EPP interface provides transmission rate from 500 KB/s to 2MB/s

- Two interfaces RS-232C provide cheap and very simple links up to 20 m in length for the maximum transmission rate of 115kbit/s. Similarly to the EPP, the RS interfaces provide integration possibilities of the controller with measurement and control apparatus and other peripheral devices of older type or enable construction of very cheap own equipment.

The peripherals of optoelectronic multi-gigabit transmission provide realization of universal connections in multi-controller configurations and building of complex networked structures of heterogeneous devices. They assure very fast, synchronous data transmission resistant to EMI, disturbances, errors, even for data transfers for long distances. Each node is equipped with two nondependent Tx/Rx circuits with exchangeable optoelectronic transceiver modules. Servicing of the signal layer and logical layer is realized in RocketIO modules inbuilt in FPGA VirtexIIPro circuit [10],

The peripheries for embedded modules enable to connect to the node two daughterboards, realized in mechanical standard PMC [19]. The communication layer embraces a standard PCI bus [20] in versions 33MHz or 66MHz and dedicated fast transmission lines LVDS configurable by the user. The controllers for both buses and electrical parameters of controlled pins are respectively implemented and programmed in FPGA circuit.

3. CONTROLLER CONSTRUCTION

The backbone PCB of the controller was designed in mechanical standard 6HE-160 (233mm x 160mm), in a homogeneous form, 12-layered, on the FR4 laminate [21]. Providing compatibility with the standard CMC/PMC [19] required positioning on the front edge of the board a 3mm cut. The cut enabled mechanical fixture for extension cards.

Seven layers of the PCB were used for the distribution of signals. The remaining five layers are devoted for distribution of power supply. From technical reasons (succession of positioning of signal layers and power supply) two external signal layers possess signal microstrip lines, two internal layers possess nonsymmetrical microstrip lines and the rest of layers possess symmetrical strip lines.

Cross section of the designed PCB for the controller was presented in fig. 2. Power supply lines distribute the following voltages: 2.5V, 3.3V, 5V and 1.5 V and 3V (as islands on the previous layers). The pile of layers possesses also two ground planes (which is a reference potential for slowly-changing signals) and a RF power return path for HF signals.

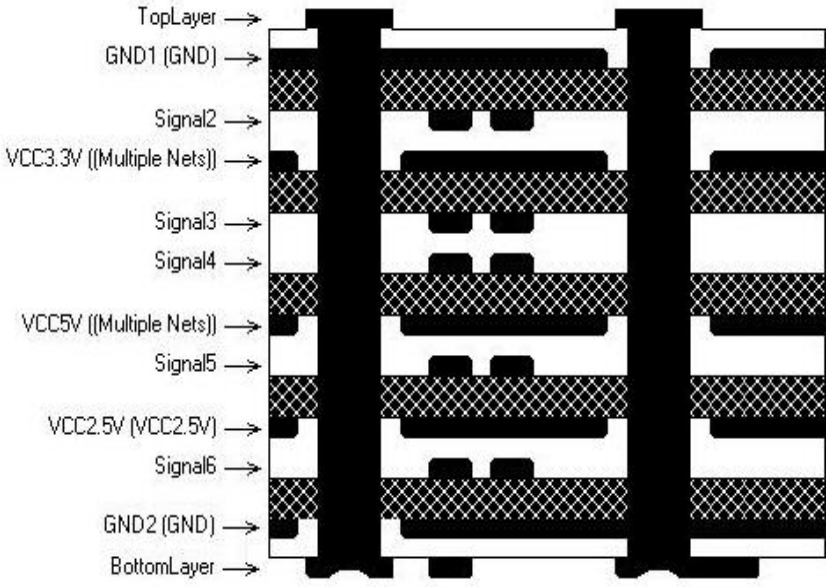

Fig.2. PCB cross section for the designed controller

The complexity of controller realization was focused mainly in the methodology of signal distribution from under the FPGA circuit, with simultaneous proper signal decoupling from its power supply circuits. The resulting topology of paths is a compromise between the following contradicting factors:

- Aiming to obtain the smallest inductances of power leads,
- Minimization of inductances of signal paths,
- Protection of topological homogeneity of bus lines.

The resulting inductance of paths, obtained during the design process, is a compromise of their effective lengths, and the number of used layers (and vias) to distribute the paths.

Contemporary digital circuits impose very high demands on power supply circuits. Power consumption is highly pulsed in the same pace as the signal clock of the control circuit. These pulses may have a value of a few Amperes taken from

the power supply during single nanoseconds. Lack of proper decoupling in the supply circuit results in generation of cyclical voltage drops on the power supply lines and propagation of these voltage pulses over the whole PCB board. In critical cases such voltage pulses may disable the whole digital system on the PCB.

In order to minimize such unfavorable phenomena, there are placed capacitors in proper places of the PCB. These capacitors support voltage value in critical places of power supply lines, where the pulse power consumption is the biggest. There are used a few levels (usually three) of power supply decoupling. The first level consists of capacitors 10 nF, and possibly low value of ESR coefficient (equivalent series resistance), which are positioned in the distance around 1cm from the supply leads of decoupled circuit. The second level are capacitors of value 100nF and positioned in the distance 4-5 cm from the circuit output pins. The third level and capacitors are of 1uF and positioned in bigger distances, possibly in a homogeneous way over the PCV. They support voltage value of the whole power supply layer in an integral way. The suggested values of capacitors for supply decoupling have approximate nature. And depend on PCB working frequency, character of controlled loads [22-24].

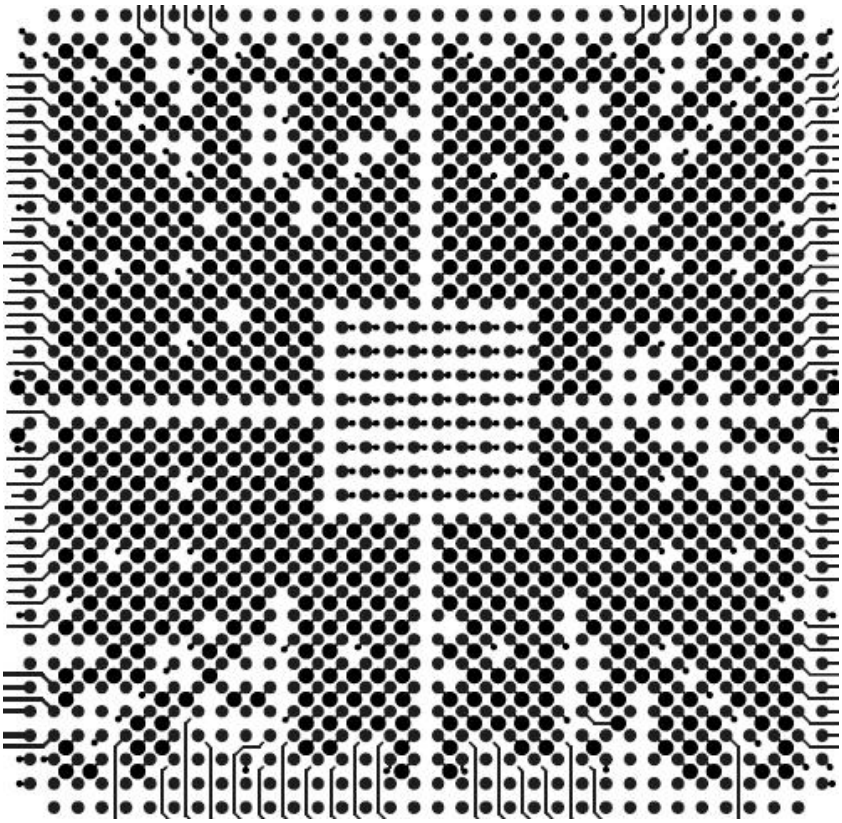

Fig. 3. Positions of soldering points and vias under FPGA circuit (Top Layer)

The methodology assumed during the design of topology of distributing paths from under a BGA circuit is called „channel routing". It creates again a compromise between the number of used I/O pins in BGA circuit, positioning of the first layer for decoupling capacitors, and the number of used layers for signal distribution. Fig.3. presents a solution assumed for realization of the controller board.

The basic confinement in the PCB design freedom during routing of signals from under the BGA circuit is critical problem of positioning of the vias and type of used vias. A basic method relies on distribution of signals by the row after row via the slots in the matrix of vias, perpendicularly to the edge of the circuit. This method is used as the most popular one in the software tools for automatic routing. This method is, however, very ineffective in the usage of the number of layers.

The controller design used the method of channel routing for signal distribution. The chosen variant of this method are two perpendicular channels, perpendicular to the chip edge and going through its center. There are no standard vias in

the channels. There was used a special advanced technique called laser microvias. The microvias have 150μm in diameter and lead from the external layers (1 and n) to layers (2 and n-1) where there are planes of ground and power supply. Due to this solution, around 25% of surface under the FPGA is appropriate for positioning of decoupling capacitors for the first layer.

An important construction feature of the controller is possibility to extend its functionality with the aid of PMC cards [19]. PMC is an industrial mechanical standard for extension cards, for connection of mother and daughterboards. It is commonly used by PCI bus PCI [20].

In the assumed solution for the controller, PCI bus uses 32 bit standard with logical levels at 3.3V, and maximum data transmission rate at 132 MB/s. Apart from commonly used PCI bus, the PMC socket gives access to 64 lines for own, special solutions. The controller used 540 out of these lines, as typical 40 I/O lines working in standard of 2.5V. The rest 12 lines is used for 6 differential signals in standard LVDS 2.5V and impedance 50 Ohm.

A considerable difficulty in construction of the controller was simultaneous positioning of two optoelectronic transceivers with double PMC socket. PMC specification predicts that from the front side of the daughterboard and motherboard, there are input/output ports of the first one and it is a prohibited area – it is impossible to position there any components (for the sake of mechanical compatibility). From this reason, the only possible solution, providing coexistence of the interfaces was positioning of the transceivers from the soldering side of the board, instead positioning them from the component side – or where the PMC socket is. The penalty price for this construction is the lack of possibility to position the controller to the slot no 1 in the VME crate, with mounted transceivers. The result is that the controller may work only in the Slave work mode.

The construction of PCB was presented in fig.4. The components marked in gray are mounted optionally. The main panel, mounted to the motherboard, possesses two blinds for PMC extension cards, Ethernet and USB sockets. From the down side (or left, in the case of positioning of the PCB in the VME crate), there are mounted optionally optoelectronic transceivers. Additionally, for the users convenience, the interfaces CAN, RS232 and EPP, with the aid of IDC ribbons and be output to an additional panel, placed next to the main board. Then, the controller occupies two slots in the VME crate.

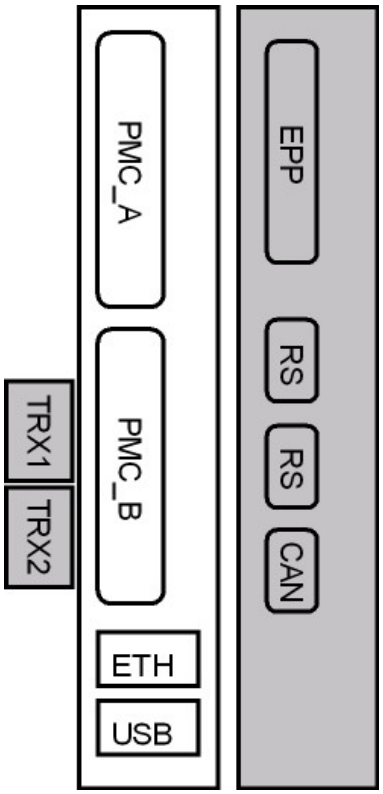

Fig.4. Front-side panel of controller

4. CONCLUSIONS

The paper presents concisely a functional idea and hardware realization of a universal, modular controller. The structural solution embraces one of the work modes as nondependent network of controllers connected by gigabit fiber optic links. Then the controller works as a network node. The construction of such a node was standardized by application of a large central FPGA circuit hosting virtually all the controller. A number of different and universal I/O communication interfaces were implemented like common interfaces (Ethernet, USB, CAN, RS-232 and others), industrial interfaces (VME, VXI), and universal PMC connectors for measurement-control interfaces.

Broadly differentiated functional requirements, which result from a particular application of the controller, are realized totally in the FPGA circuit. There was provided an easy method of multiple reconfiguration of FPGA circuit in order to provide application of the same network node in different work topologies with a variety of different measurement and control devices.

Exchangeability of control and measurement devices which cooperate with the measurement network node stems from the usage of daughterboards inserted to PMC connectors or with connections of particular devices to particular communications ports of the node. This situation of the node work mode was presented in an application example in chapter 4. Adaptation of the required functionalities for servicing of a variety of control and measurement equipment and devices in primarily realized in the programmable FPGA circuit.

To be able to use the controller board in industrial conditions, with usage of the VME/VXI standard, the PCB was manufactured in EURO-6HE-160 mechanical standard. This solution enables integration of the controller with other commercial modules or with the supervising system of industrial crate control. The VME-bus interface implemented in FPGA chip enables application of the node as a crate controller and further the integration of controller with modules present in this crate. Application a separate power supply connector on the PCB makes out of it an autonomous system which may be positioned in other devices or enables its work as a standalone device.

5. ACKNOWLEDGMENT

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