FPGA based Multichannel Optical Concentrator SIMCON 4.0 for TESLA cavities LLRF Control System

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ABSTRACT

The paper presents an idea, design and realization of a gigabit, optoelectronic synchronous massive data concentrator for the LLRF control system for FLASH and XFEL superconducting accelerators and lasers. The design bases on a central, large, programmable FPGA VirtexIIPro circuit by Xilinx and on eight commercial optoelectronic transceivers. There were implemented peripheral devices for embedded PowerPC block like: memory and Ethernet. The SIMCON 4.0 module was realized as a single, standard EURO-6HE board with VXI/VME-bus. Hardware implementation was described for the most important functional blocks. Construction solutions were presented.

Keywords: Free Electron Laser, accelerator, super conducting cavity, cavity controller, photonic system monitoring, VHDL, Xilinx, SIMCON, SIMCON 4.0, Low Level RF systems, LLRF,

1. INTRODUCTION

Stable work of a resonant high power superconductive cavity, which is a device for elementary particle acceleration, requires high EM field stability, i.e. its phase and amplitude. Stabilization of cavity work conditions relies on controlled, dynamic changes of provided power. This is performed in the LLRF (Low Level Radio Frequency) control system which works in a feed back loop [1,2]. A multilayer structure of LLRF control [8] for linear accelerator propelling the FEL is presented in fig. 1. The used cavities are of TESLA Technology type [4].

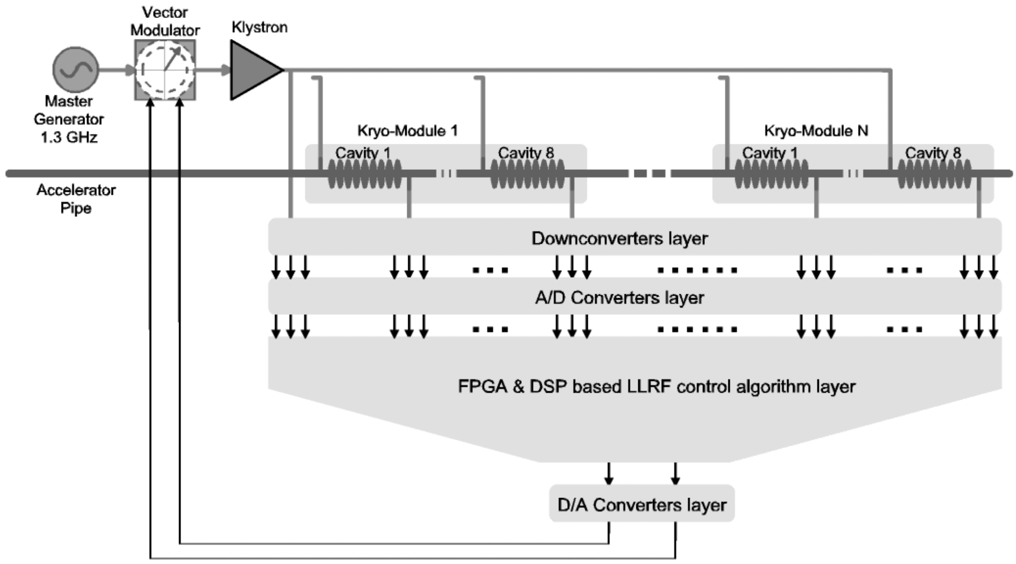

Fig. 1. General diagram of LLRF control system for FEL accelerator.

The role of electronic control system is to stabilize the high power accelerating, electrical field in the resonator at a cost of the smallest possible exciting power. The measured 1,3GHz signals from the cavities are down-converted in frequency to 250 kHz in respective blocks, maintaining all information about the phase and amplitude of the field. The signals, after ADC, are input to the digital part of the control system. Fast phase and amplitude control of the accelerating field is realized in the feedback by DSP algorithm [5]. Klystron control is done via vector modulator.

Speed of the system, and especially the clock rate of DSP, is the most important factor influencing the quality and stability of the beam. With the speed in mind, there were undertaken research efforts to built LLRF generation of control systems basing on the fastest and the largest FPGA chips, containing considerably large number of DSP blocks 6], logical circuits, large blocks of internal RAM memory, modules of multi-gigabit optoelectronic transmission, standardized communication interfaces, etc. These resources enable not only implementation of all needed LLRF functionalities but also diagnostic layer and fast communication interfaces.

This research on future and optimal LLRF system aims at lowering the latency, increasing the number of available channels, and obtaining universal and scalable system structure [7,8,3]. The LLRF systems from the side of data flow and processing may be considered as a large, multichannel, synchronous, pipeline, functional, fig. 1. Multichannel ability is caused by a large number of cavities to be controlled simultaneously but nondependently. Individual cavity control requires nondependent readout channels. Synchronous character of the system defines precisely the system time and data processing for the same accelerator pulse. Pipeline character of the system enables step by step data processing in a very complex architecture. It provides data resolution for complex DSP and system time.

Fig. 2 presents a general hardware distributed model of LLRF system basing on FPGA circuits interconnected by an optical network [9]. This solution enables relatively easy system structure modification, change of the number of active channels, change of features and functions of DSP. Networked character of the system requires, in case of need, its partial changes and reconfigurations in critical parts only, without changing its general topology.

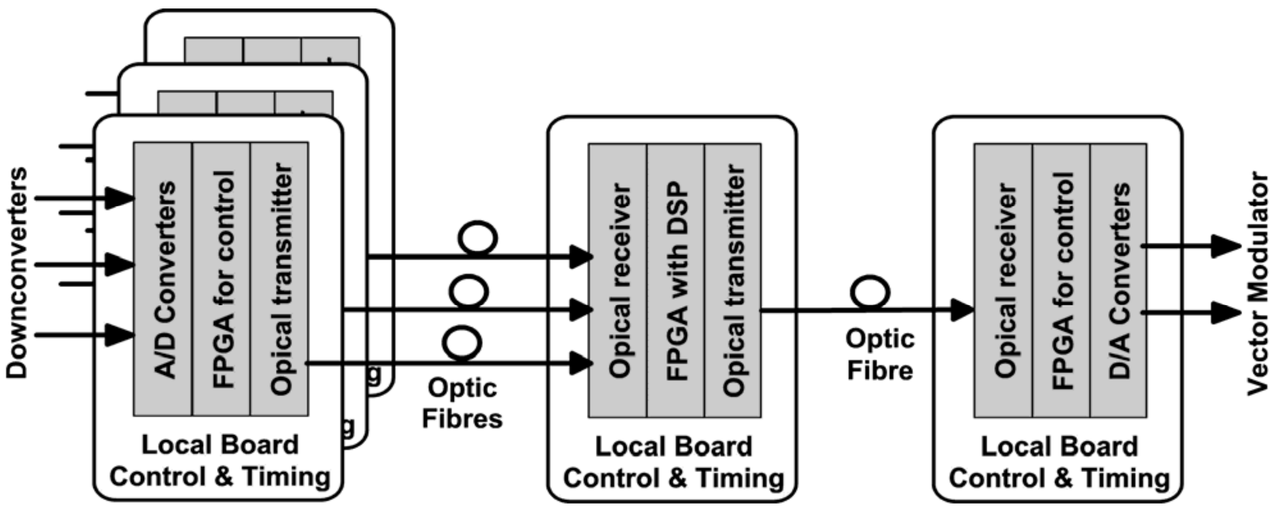

Fig. 2. General diagram of LLRF control system for FEL accelerator.

The tasks for functional concentration stem from DSP algorithms, which calculates the results for many channels, basing on input data and set point. These tasks may be realized in a distributed form, step by step (multistage process) or concentrated in a single, very efficient FPGA/DSP circuit. The hardware concentration is a consequence of functional concentration. Many physical signals are concentrated in a single object of complex numerical processing. This paper presents a designed and then realized complex functional and thus hardware data and DSP optoelectronic concentrator for LLRF system of FLASH.

2. FUNCTIONAL STRUCTURE OF LLRF CONCENTRATOR

This chapter discusses the most important functional blocks of LLRF functional and hardware concentrator, called SIMCON 4.0. The SIMCON receives signals from TESLA resonant superconductive cavities. The signals are: field probe, forward and reflected power. Block diagram of the system was presented in fig.2.

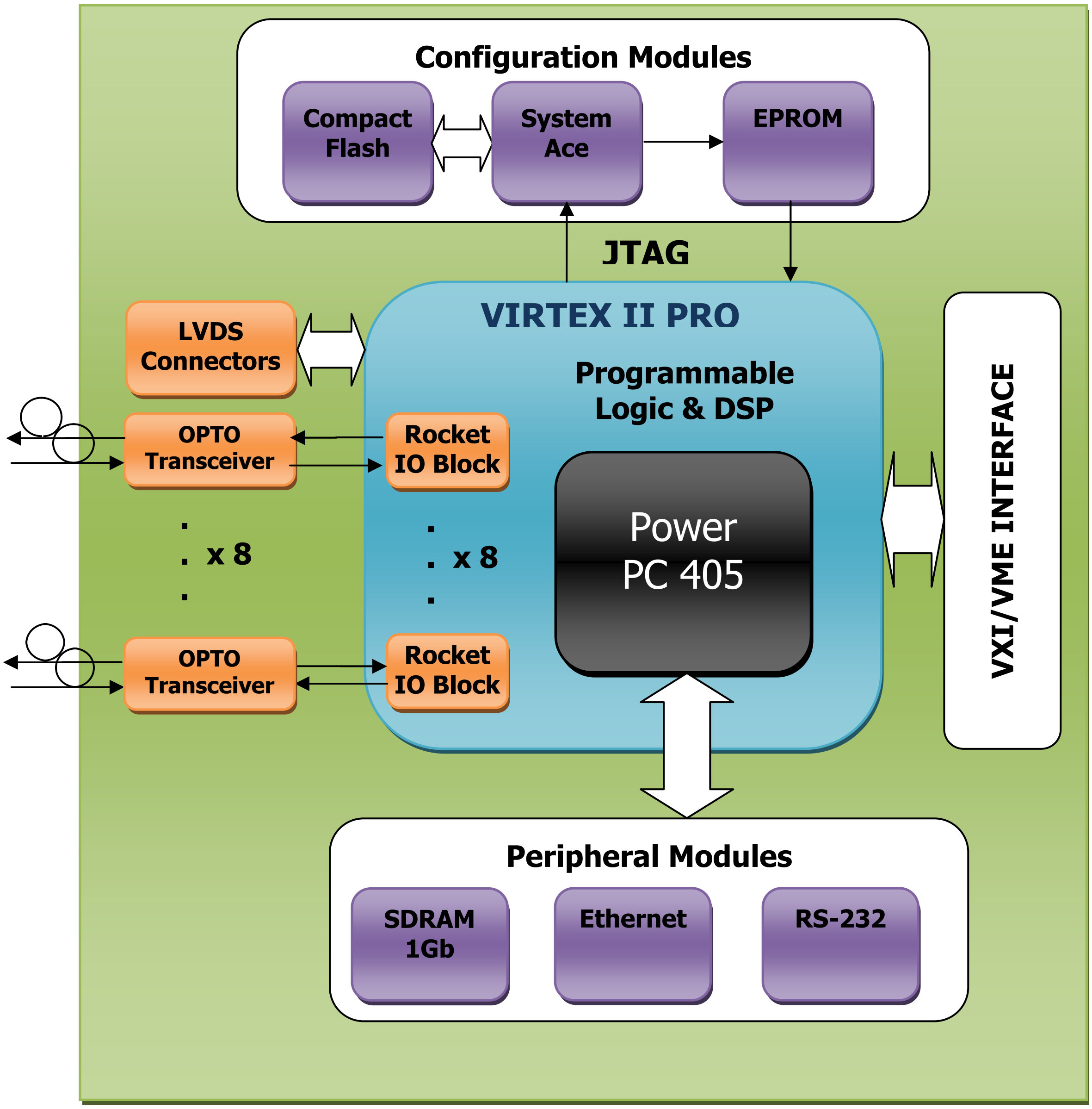

Fig. 3. General diagram of LLRF control system for FEL accelerator.

The heart of SIMCON 4.0 is FPGA Virtex-II-Pro [10]. The circuit is equipped in internal hardware blocks cooperating with programmable internal logical blocks:

- RocketIO™ with inbuilt Multi-GogabitTransceivers (MGTs) [11]
- processors RISC IBM PowerPC™ 405 [12]
- configurable blocks of SRAM memory and block SelectRAM™
- dedicated, fast multiplication blocks 18x18 bits
- dedicated DCM circuits for distribution, phasing and conversion of clock frequencies,

• digital control of I/O impedance.

The inbuilt RocketIO blocks provide hardware based, serial, two directional data transmission with the rate over 2Gbps, optimal synthesis of clock signal for transmission, clock signal recovery from received signal. The blocks support 8B/10B and 64B/66B coding, automatically regulate signal level from 200mV to 1600mV and provide compatibility with voltage levels for other serial transmission systems. Each pair of I/O ports has termination with 50Ω or 75Ω. The largest Virtex II Pro circuits possess up to 16 nondependent RocketIO blocks.

The inbuilt 32-bit processors IBM PPC405 [12] may work with frequency 250-450MHz depending on version of the chip. Dedicated applications were launched under Linux MontaVista. The applications included: control, monitoring, diagnostic, management, etc. Implementation of a standard operational system provides additionally a series of useful tools to administer the system, manage standard interfaces (like Ethernet), and numerable user packets of software. Depending on the type of FPGA Virtex II Pro circuit, it is possible to use one or two IBM PPC405 processors working in parallel.

Tab.1 gathers basic parameters of XC2VP50 [10] from Virtex-II-Pro Xilinx family of chips, which was implemented in SIMCON 4.0 hardware concentrator.

RocketIO Transceiver Blocks	*PowerPC Processor Blocks*	*Logic Cells*	*CLB (1 = 4 slices = max 128 bits)*		*18 X 18 Bit Multiplier Blocks*	*Block SelectRAM+*		*DCMs*	*Maximum User I/Slices O Pads*
			Slices	*Max Distr RAM (Kb)*		*18 Kb Blocks*	*Max Block RAM (Kb)*		
16	2	53,136	23,616	738	232	232	4,176	8	852

Tab.1. Basic parameters of chip XC2VP50 Virtex-II-Pro Xilinx

To realize SIMCON 4.0 concentrator board, there were used rich resources of Vitexa II Pro family included in the XC2VP50 chip and external additional auxiliary components and peripheral devices. The SIMCON 4.0 board was equipped in the following functional blocks:

1) Integrated initialization, booting and configuration block: contains JTAG link [13], EPROM circuit [14] and SystemACE circuit [15]. JTAG link is a low level, standard interface of general use, designed for configuration and communication with FPGA chip via external devices and a computer. There are connected to JTAG chain other configuration circuits and cooperation between them was established.

   32Mb EPROM XCF32P chip was applied for fast and automatic configuration of FPGA XC2VP50. EPROM is connected with parallel bus to FPGA. Slave SelectMAP mode of work was used to minimize the initialization process time.

   Implementation of chipset *SystemACE – XCCACE* which realizes communication with *Compact Flash* cards, extends considerably the possibilities to automatically configure FPGA chip and inbuilt IBM PPC405 processor. System ACE provides a complex initialization of FPGA circuit. FPGA is configured and *Compact Flash* card is mounted (the card works in mini-disc mode), a system of files is also mounted, appropriate for the launched operational system. The memory card is also used as a universal mass memory for the operational system, measurement data recording for LLRF system, and configuration data provider for LLRF controller.

2) Multi-channel optical interface: contains eight nondependent, two directional channels of multi-gigabit, synchronous serial data transmission [11]. It is the most important communications interface on SIMCON 4.0 concentrator PCB. Infineon V23848-M305-C56 optoelectronic transceivers were used. They provide data transmission with the rate up to 2.125Gb/s in both directions. Multimode optical fibers were used for 850nm of optical wavelength. The maximum length of data distribution in optical network connecting other SIMCON 4.0 and SIMCON 3.1 nodes is predicted not to exceed 200m.

   The transcievers were connected directly to eight nondependent RocketIO blocks inside VirtexIIPro XC2VP50. The full process of serialization, deserialization, coding and decoding of data stream and integration with the rest of programmable logic, is fully realized inside FPGA. The Rocket IO blocks are supplied from separate low noise circuits TPS78625 by Texas Instruments in order to minimize the overall noise performance of the SIMCON system.

3) Peripheral devices cooperating with IBM PPC405 processor provide installation of a full operating system with required tools, communication layer, and usersoftware. The SIMCON 4.0 PCB was equipped with 1GB (128MB) SDRAM memory, and communication links (Ethernet 10/100Tb and RS-232).

Application of MT48LC4M16A2-7E circuits working with 133MHz frequency, enabled installation of Linux on PowerPC processor with the necessary software packets and provided efficient work for at least a few parallel processes and services.

Ethernet is a fundamental communication layer for PPC processor with other external devices and computer network. The physical layer of communication is serviced by Broadcom BCM5221 chip. It provides connections in 10/100Mb/s standard on 4-pairs class 5e cable. Choice of this particular chip was dictated by availability of drivers for this particular distribution of Linux. Linux has a full control over BCM5221 and services the logical layer of Ethernet transmission.

Terminal RS232 link was realized using MAX3232 circuit. A standard channel for operator console was obtained. It provides system control on the lowest level. Processor status can be traced via the console. Orders can be issued via the console.

External memory, Ethernet link, RS232 link are accessible for the programmable logic of FPGA, and may be used alternatively in other implementations of the hardware.

4) VXI/VME-bus communication interface: [16] provides integration of SIMCON 4.0 concentrator board with the hardware control environment of LLRF (like other boards, SIMCON 3.1 [3], SUN computer, etc.) and programming layer DOOCS [17]. In such a configuration, SIMCON 4.0 is placed in VME 6HE crate and may work in „slave" mode A24D32 or A32D32.

The designed VME interface provides also the „master" work mode ability and then SIMCON 4.0 is a crate controller. Two double-directional buffers IDT74FCT164245 were used. They play a role of current buffers cooperating with VME-bus, convert voltage levels from 5V on VME to 3.3V for FPGA, provide change in data direction flow. Control of data direction flow for particular groups of buffers is realized in FPGA. It enables implementation of advanced VME controller.

The buffers are also connected to the lines LBUSA and LBUSC to obtain additional, fast parallel user buses, on the backplane, to work with VME interface. In the case, the system uses VXI interface, these lines are part of the system bus.

5) Configurable LVDS links: are dedicated for fast data transmission between neighbouring boards. There were used two SAMTEC connectors, providing maximum data rate of 2Gb/s. The connectors are linked directly to FPGA pins. It provides configuration of particular signals (standard choice electrical LVPECL or LVDS, data flow direction, etc.). There is predicted space for external termination predicted for differential transmission standard LVPECL.

6) Synchronization clocks: for subsystems RocketIO, SystemACE, initialization EPROMu, and FPGA with embedded PowerPC processor. Two clocks are on the board of 106,125MHz to service eight used RocketIO channels. Two nondependent quartz generators were predicted for FPGA applications 60MHz or 80MHz. There was implemented clock signal 33MHz to cooperate with SystemACE and PPC. Clock 40MHz is used for loading configuration into FPGA from EPROM'u. The controller is equipped in four SMA connectors for input clock signals and trigger signals synchronizing the work of concentrator with the rest of the LLRF system.

7) Power supply circuits: require connection of a single 5V power supply unit. They provide the following five voltage levels:

- 5V is for supply of buffers from VME bus side,
- 3.3V is used for powering of: VME interface form FPGA side, SDRAM memory, switches and LED as well as appropriate banks of FPGA XC2VP50 circuit,
- 2.5V supplies external modules of optoelectronic transceivers, SystemACE circuit and appropriate banks FPGA XC2VP50,
- 1.5V is for supply of FPGA XC2VP50 circuit core,
- -5.2V is only for supply of control ECL buffer on VXI bus.

3. CONSTRUCTION OF OPTOELECTRONIC CONCENTRATOR SIMCON 4.0.

SIMCON 4.0 system was realized in a form ofa single 6HE-160 PCB, what provides VME crate compatibility. The board was designed according to „RoHs" directive, which avoids usage such elements as lead, mercury, cadmium, chromium for manufacturing of electronic devices. It forced usage of special laminates withstanding higher soldering temperatures, for lead-free PCB technology.

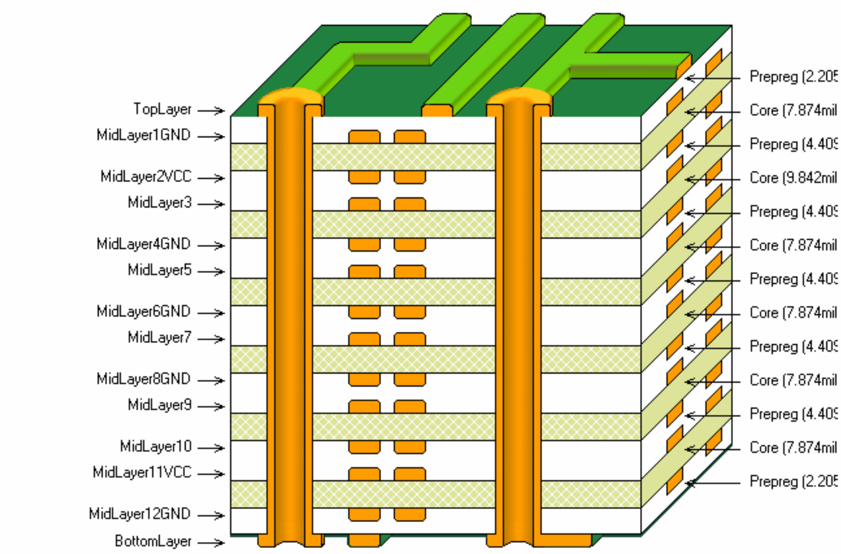

Fig. 4. Cross section through SIMCON 4.0 PCB

SIMCON 4.0 PCB has 14 layers. Cross section of this PCB was presented in fig. 4. Usage of relatively large number of layers stems from the necessity to connect over 1000 pins of FPGA to the external components and observing all proper engineering rules of PCB design, like layer distribution for constant electrical potential. It is extremely important to distribute properly the power supply layers for shielding purposes and impedance stabilization for the layers with differential transmission lines. The differential lines are present in the following layers of SIMCON 4.0. Top, Mid3, Mid5, Mid7 and Mid9. These layers were positioned in between layers of constant potential, which resulted in the decrease differential line thickness and separation between them.

The PCB design was done in 5mil technology, for the path thickness and for path separation. It resulted in effective paths distribution, especially from under FPGA circuit. The necessity to make vias of small dimensions increases the impedance. This effect is especially important for supply lines. Keeping the noises, for power supply lines of FPGA core below the maximum allowable level of 25-35mV, to provide its proper work, required supply lines to go via capacitor pads, what was presented in fig. 5.

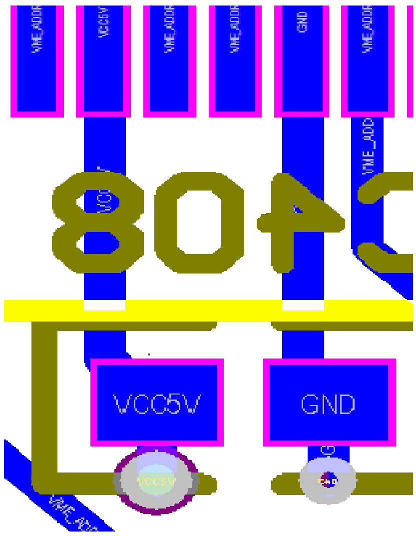

Fig. 5. Example of paths distribution between pads of capacitor

Large surface of PCB requires potential equalization between layers of the same supply level. In particular it concerns the ground layers (GND). In order to provide this, a large number of distributed vias were used between the ground and equipotential layers. In particular it concerned the areas around the transceivers and FPGA, where a high stability of power supply levels is required. Each power supply layer contains "commas" in order to direct the current flow and eliminate harmful eddy currents.

The components on the SIMCON 4.0 board were positioned centrally around FPGA circuit, to minimize the lengths of interconnections and provide homogeneity in pins distribution in particular blocks of FPGA banks. Fig. 6 presents distribution of components on the upper layer.

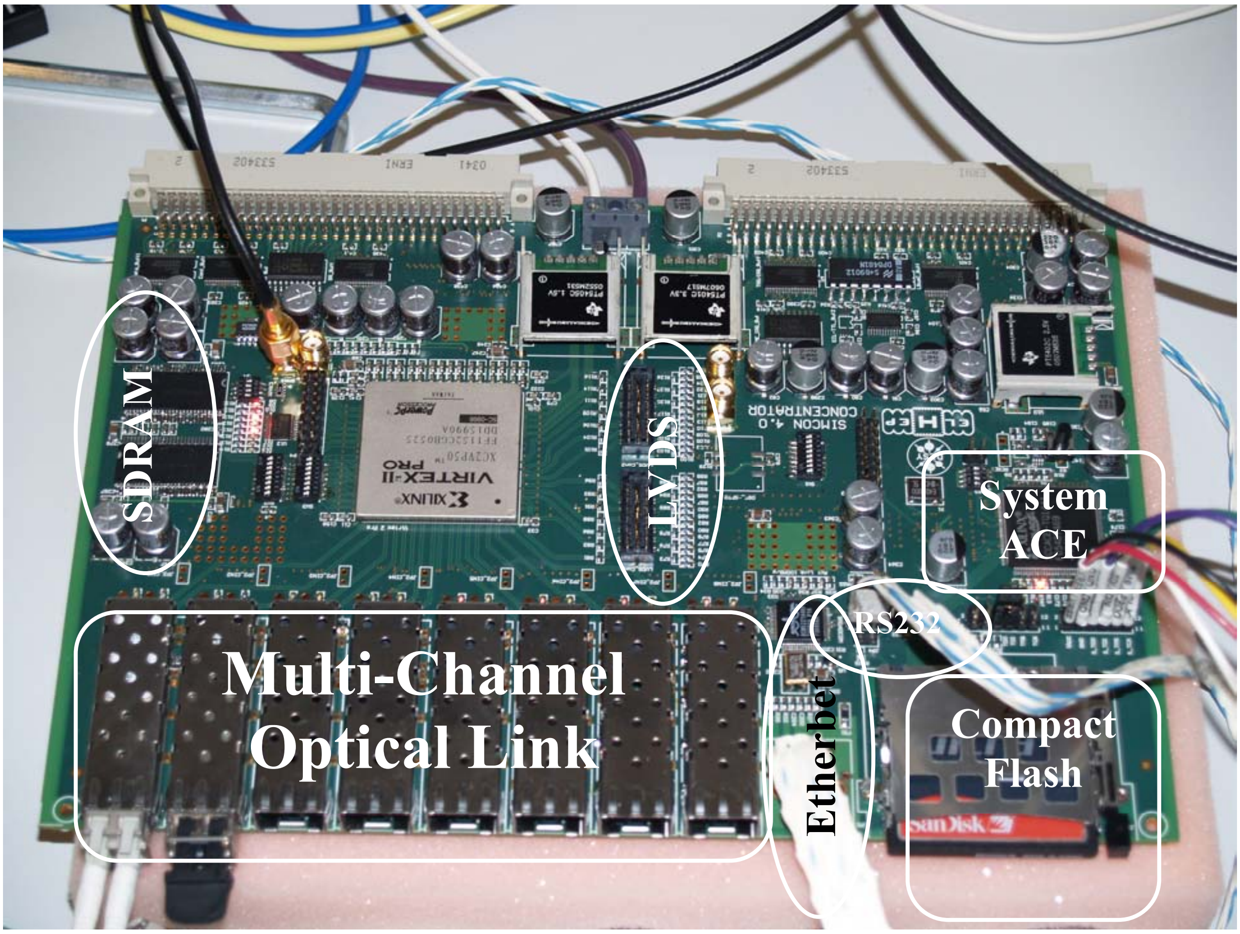

Fig. 6. Photograph of upper side of SIMCON 4.0 PCB

FPGA circuit was positioned symmetrically against the connectors for optoelectronic transceivers. Optimal choice of RocketIO enabled realization of short and resistively stable connections for gigahertz signals. Peripheral components, which require fast communication (for example, SDRAM memory, LVDS connections, etc.) were placed nearby FPGA. Alternatively, the circuits for FPGA configuration and communication were positioned further away from FPGA circuit.

Front panel of the SIMCON 4.0 board gives access to eight connectors of optoelectronic transceivers, Ethernet connector 10/100TB and CompactFlash mini-dics connector. The rear side of SIMCON 4.0 PCB possesses standard VME/VXI-bus connectors. SIMCON 4.0 occupies a single slot in VME crate. Additional connectors were predictedon the board (RS-232, synchronization signals). These connectors may also be transferred to the front panel of the double width.

4. CONCLUSIONS

The paper presents shortly a functional idea and hardware realization of a universal, programmable, optoelectronic concentrator SIMCON 4.0 predited for work as a part of LLRF control system in FLASH accelerator and laser. The system cooperates with SIMCON 3.1. boards and controls the field stability in superconductive, resonant, microwave, TESLA cavities. A large variety of functionalities of SIMCON 4.0 PSC is realized in programmable FOGA chip with the usage of internal DSP blocks. Additionally, a number of peripheral devices were positioned for internal PPC processor like SDRAM memory, Ethernet connection, etc. The PPC is used for monitoring processes, management system calibration, etc. Implementation of VXI/VME interface enabled connection of SIMCON 4.0 concentrator to the DOOCS control environment, which is used for FLASH control.

Integration of SIMCON 4.0 concentrator with eight SIMCON 3.1 boards via multi-gigabit optical network results in a homogeneous control system equipped totally in 80 measurement and control ADC channels and 24 DAC channels. The system promises for a universal, scalable, distributed hardware solution. Application of fast optical links enabled big scale of channel concentration in a single FPGA circuit with the latency of the order of 200ns.

Now there are continued advanced application tests of SIMCON 4.0 system in FLASH laser. This test work embraces: realization of control algorithm for 16 resonant cavities powered by a single klystron. SIMCON 4.0 provides readout of field probe values, as well as forward and reflected power.

There is also realized a project to implement SIMCON 4.0 for a central monitoring of signals from the whole FLASH accelerator and laser for calibration, monitoring, diagnostics, exception handling slow and fast control, and cooperation with other systems, like beam diagnostics, interlocks, etc. SIMCON 4.0 opens really a completely new field of control reach for LLRF systems for the next generation of accelerators and light sources.

5. ACKNOWLEDGEMENTS

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