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Modular & reconfigurable common PCB-platform of FPGA based LLRF control system for TESLA Test Facility

Krzysztof T. Pozniak, Ryszard S. Romaniuk
Institute of Electronic Systems, Nowowiejska 15/19, 00-665 Warsaw, Poland
Krzysztof Kierzkowski
Institute of Experimental Physics, Hoza 69, 02-093 Warsaw, Poland

ABSTRACT

The paper includes a description of predicted functionalities to be implemented in a universal motherboard (MB) for the next generation of LLRF control system for TESLA. The motherboard bases on a number of quasi-autonomous embedded executive modules. The modules are implemented in a few FPGA chips featured by the MB. The paper presents a practical design of the MB. The initial (basic) solution of the MB has the Cyclone as the chip where the board management is embedded. The board features communication modules – VME and micro, single chip PC with Ethernet. The board provides power supply for the FPGA chips. The board has fast internal communication between particular modules.

Keywords: Super conducting cavity, FPGA, VHDL, Ethernet, VME, Altera, Xilinx.

1 INTRODUCTION

The mother PCB for the next generation LLRF control system (LLRF-MB) should be a universal, modular and reconfigurable platform to accommodate a number of specialized functional modules. It is assumed now that the modules base on the programmable FPGA chips of sufficient resources (fast clock, fast FIFOs, large enough memory, DSP blocks, large number of LCELLs, large number of I/O ports). It is also assumed that the external communication to the LLRF control system is provided by very fast optical links. Such an assumption allows to extract common components existing inside the LLRF control system. Extraction of common components avoids repetition of the same functionalities in different modules throughout the system. The repetition results in resource losing and performance decreasing. The identification and extraction of common functionalities in the system results in considerable simplification of the hardware and allows for parameterization and standardization of software control modules. The design process embraces narrower extent of functional requirements. The parameterization of common functional blocks makes the design more flexible, thus, saving the labor time and project costs.

The general functional block diagram of the common hardware platform was presented in fig. 1. The LLRF SC cavity control platform consists of the following components:

1. The major and central component is *PLATFORM CONTROLLER (PC).* The tasks of the *PC* are:
   - communication with standard external I/O interfaces;
   - internal communication with particular functional blocks;
   - distribution of fast control and synchronization signals among the blocks and to/from the external parts of the system.

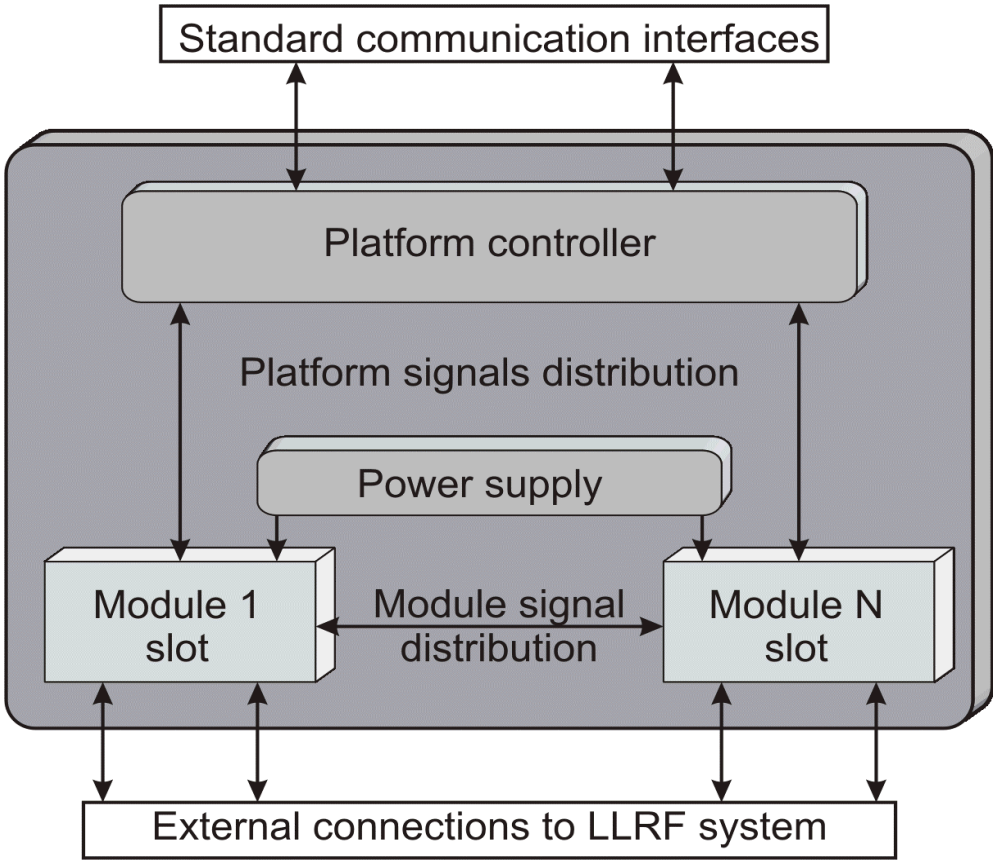

Fig. 1. General idea of the, FPGA based, hardware platform for the next generation LLRF control system for TESLA.

2. The particular slots of the functional blocks have fast direct connections with the rest of modules. This solution provides synchronous work of particular modules and fast data exchange, checking, operator's and control signals exchange.
3. A common power supply system provides the slots with typical voltages required for contemporary FPGA chips, drivers, converters, and analog components.
4. The integration (of the blocks residing on the LLRF MB) with the external parts of the LLRF control system is realized via the *EXTERNAL CONNECTION* blocks positioned on particular modules. Such a solution provides separation between the general platform structure from the current configuration of the LLRF system realization. The changes in the LLRF system concern only modification of a few particular functional modules (not the whole LLRF MB).

2 FUNCTIONAL STRUCTURE OF THE LLRF CONTROL PLATFORM FOR TESLA EXPERIMENT

The universal hardware platform designed for the LLRF control system [1,2] was adapted to the key requirements of the TESLA (test facility) experiment. The possibility to control the system via the VME bus was provided [8] as well as the operator's access and computer network control via the DOOCS [9]. The platform takes also into account the system clock timing and very stable reference signal distribution throughout the whole distributed experiment resources. The distributed modules have to work in the synchronous regime.

Fig. 2. shows functional structure of the hardware platform for the debated, FPGA based LLRF control system. The block of *PLATFORM CONTROLLER* consists of three cooperating modules:

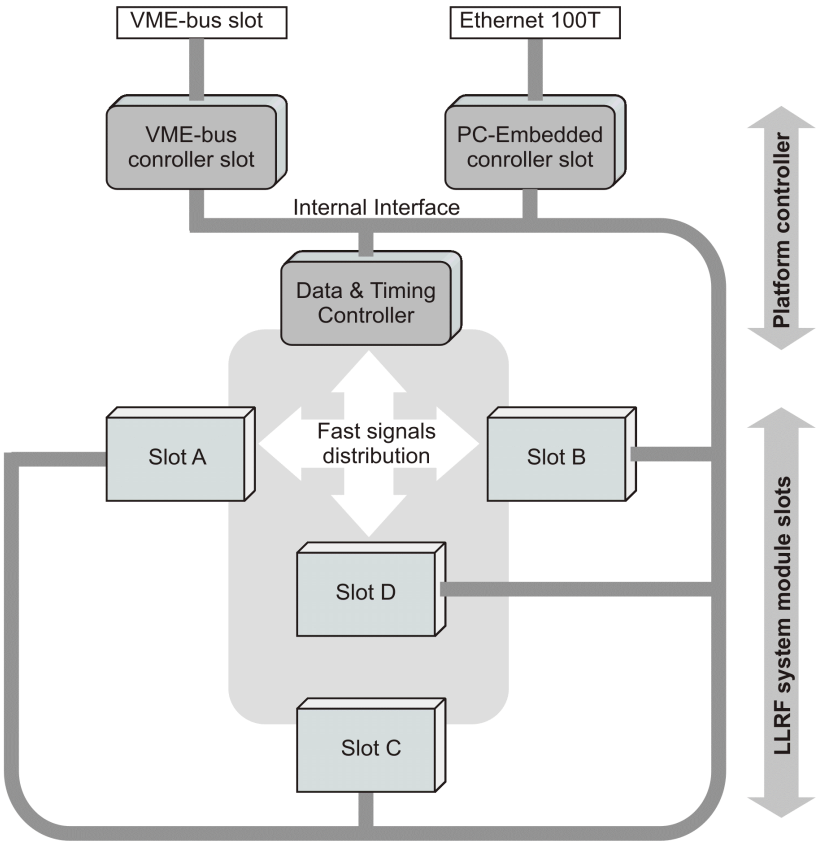

Fig. 2. Functional structure of the FPGA based hardware platform for the LLRF control system.

- The VME bus standard communication is realized by the module *VME-BUS CONTROLLER* (see paragraph 3.1). It is a passive control variant, where the whole supervision over the LLRF is done by the external controller. This solution provides integration of the hardware platform for LLRF and all functional modules with the DOOCS programming environment [9]. The control is provided by the SUN-SPARC computer, which has the VME controller.
- The active control method is provided by alternative (optional) communication module *PC-EMBEDDED CONTROLLER* (see paragraph 3.1). Implementation of a PC class computer (either single chip with embedded OS – in hardware solution, or totally software based - like NIOS) enables realization of the complex checking and control operations over the LLRF and signal processing, hardware and data monitoring and data acquisition. The standard Ethernet port is used to communicate with the external monitoring and supervision systems and between particular platforms of the LLRF system [4,7].

The module *DATA & TIMING CONTROLLER* provides global distribution of very fast synchronizing signals (see paragraph 3.3) and data (see paragraph 3.4) to all the slots. The distribution system was implemented in the programmable chip. Thus, its functionality and extent of the internal programming may be modified depending on the current requirements of the LLRF system and functional modules configuration in the slots of the hardware platform.

The communication inside the platform, among the modules (see paragraph 3.1) is realized by the proprietary standard *INTERNAL INTERFACE* [3,6]. The modules *VME-BUS CONTROLLER* and *PC-EMBEDDED CONTROLLER* fulfill the roles of communication bus controllers (“master”). The rest of the modules and slots work as “slave”.

The communication layer of the platform with the external computer system provides

programmable configuration mechanisms for FPGA chips which are situated on the platform (see paragraph 3.2) and placed in the slots **A** - **D**.

The platform possesses four universal user slots designed for functional modules. The slots **A**, **B** and **C** are configured in a parallel way, i.e. peer to peer, but the slot **D** was configured as the central one. The direct signal connections are provided between the slots. They enable transmission of fast synchronizing signals (see paragraph 3.3.) and data (see paragraph 3.4).

3 HARDWARE PLATFORM FABRICATION FOR LLRF CONTROL SYSTEM

The hardware platform for the LLRF control system was realized as a multilayer PCB of the EURO-6HE standard. The board has standard two P1 and P2 VME-BUS connectors [8]. Fig. 3. presents the front side of the of the board, while fig. 4. its rear side.

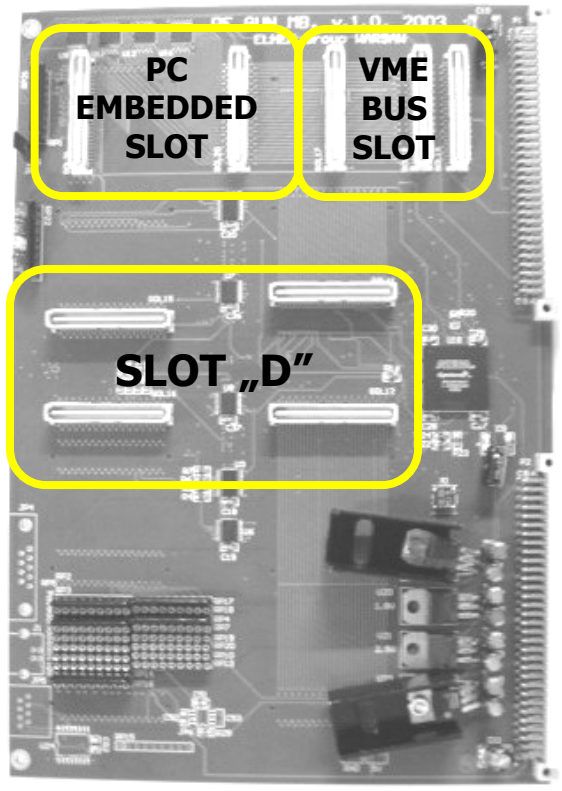

Fig. 3. Front side of the hardware platform for the LLRF control system.

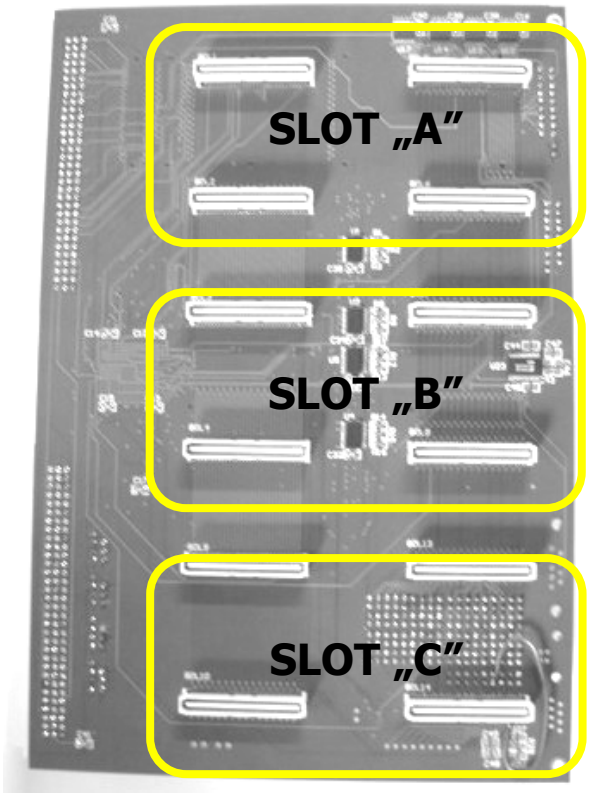

Fig. 4. Rear side of the hardware platform for the LLRF control system.

The front side of the platform PCB contains:

- Slots for daughter boards (MODULES) for communication *VME-BUS CONTROLLER* and *PC-EMBEDDED CONTROLLER*;
- Module *DATA & TIMING CONTROLLER* implemented totally in the FPGA matrix CYCLONE by Altera;
- Block *POWER SUPPLY* consists of a few nondependent resistive voltage stabilizers . The PS module provides the following voltages: 1.5V, 1.8V, 2.5V, 3.3V
- Connectors for the VME-BUS (*J1* i *J2*), connector *RS-232C* (to the terminal of PC-EMBEDDED), socket *ETHERNET 100T* and *USB 1.0*.
- Slot for the **D** module.

The rear side of the platform PCB features **A**, **B** and **C** slots.

3.1 Tiers of the computer communication system

The computer communication system is realized as a double level system, what was presented in fig. 5. The first level embraces modules *VME-BUS CONTROLLER* and *PC-EMBEDDED CONTROLLER*, which work as "master" devices. They realize the conversion of appropriate commercial communication standards to the second layer. The second layer is realized by INTERNAL INTERFACE [3]. The II provides internal communication in the "slave" work

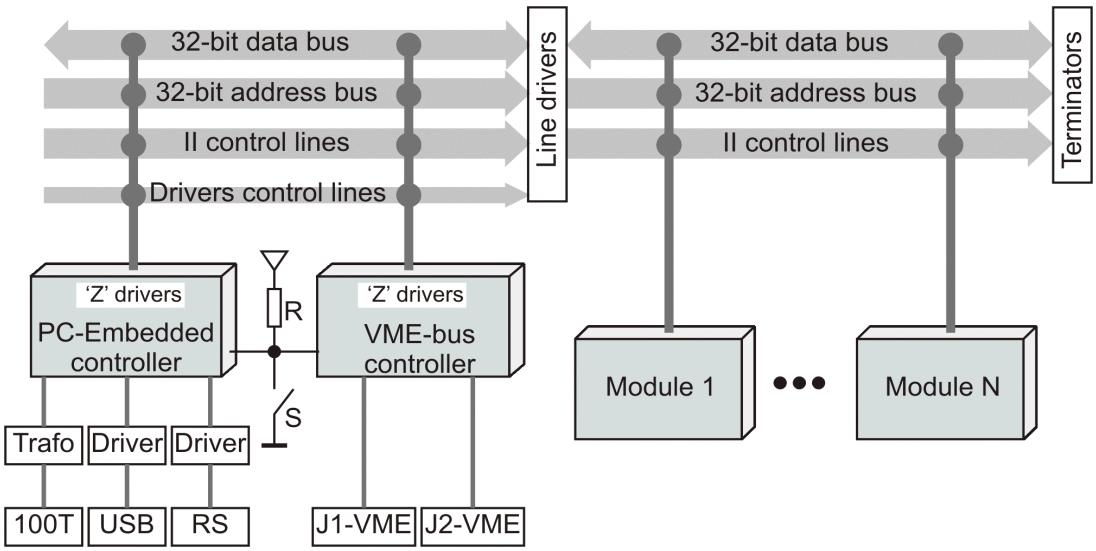

Fig. 5. Functional structure of the two layered computer communication system.

regime with all the functional modules of the platform positioned in slots **A** - **D**.

The implemented version of the INTERNAL INTERFACE standard includes 32-bit data bus, 32-bit address bus and set of lines managing the communication. From the PC control network side, the INTERNAL INTERFACE bus opens the address space and data space and enables access cycles for each "slave" module positioned on the hardware platform for the LLRF. The choice of the individual address space is done by recognition of a unique identification number for a slot: **A**=*0*, **B**=*1*, **C**=*2*, **D**=*3*. The identification number is determined by two set logical states transmitted by separate link to the slot connector. The drivers working as „master" are connected in parallel to the INTERNAL INTERFACE bus by three-state buffers (*'Z' DRIVERS*). The choice of active driver is done on the basis of arbitrating line logical states. The state may be set by the user using the "S" switch or automatically by the cooperating drivers.

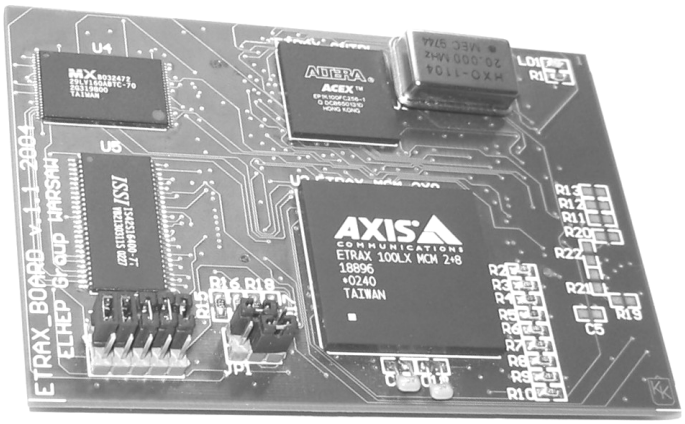

Fig. 6. Controller module PC-EMBEDDED

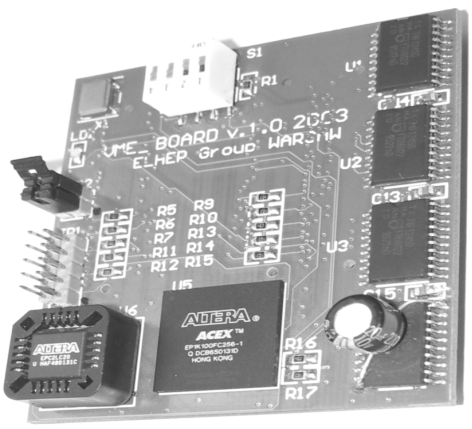

Fig. 7. Controller module VME-BUS

The controllers of the INTERNAL INTERFACE bus are situated in dedicated slots. They can be exchanged for newer versions or the ones with more functionalities. The base board contains only the necessary sockets and connectors and standard interfacing circuits (see fig. 5).

Fig. 6 presents the *PC-EMBEDDED* module, which is used at the moment [7]. The module is realized using a single chip PC (ETRAX 100 XL). The ETRAX is equipped in Ethernet 100T, USB 1.0, and RS-232 interfaces to communicate with the terminal. The embedded PC operates under the Linux OS. The hardware communication converter was implemented in the FPGA chip ACEX 100K by Altera [10]. The programming (configuration) of the FPGA matrix is realized by ETRAX chip.

The controller of VME-BUS, which is shown in fig. 7 was realized in the FPGA ACEX 100K matrix chip by Altera. The FPGA chip is configured automatically with the aid of the EEPROM memory just after switching on the power supply. The module services the „*slave A24-D32*" work mode of the access to the VME bus. The 4-bit base address of the module is equivalent to the base address of the hardware platform for the LLRF system. To obtain the range of 32 bits of the address in the internal bus INTERNAL INTERFACE is done via the usage of the paging mechanism.

3.2 Hierarchical configuration of FPGA chips

Application of FPGA matrices enables multiple modifications of the LLRF system functionalities, without the need to do any hardware changes. Fig. 8 presents (from the functional side) the hierarchical configuration of the FPGA chips realized on the debated hardware platform.

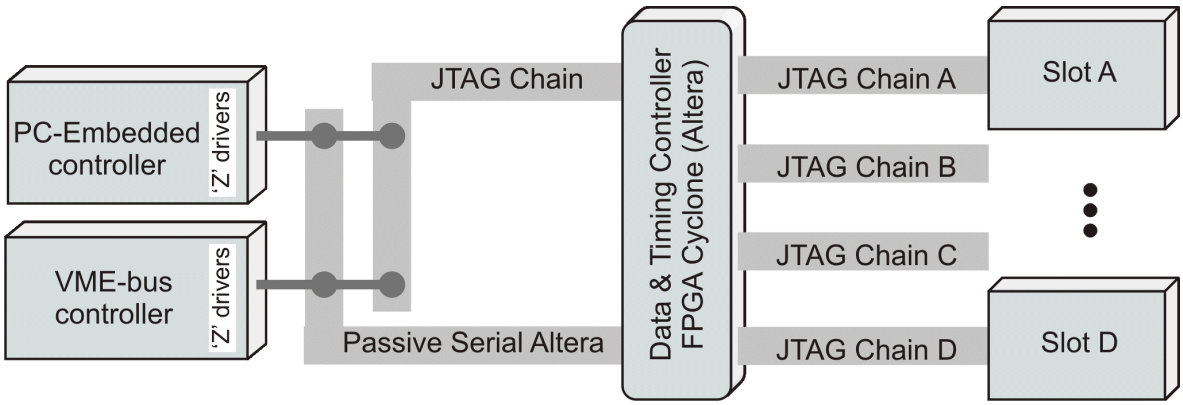

Fig. 8. Functional structure of the hierarchical configuration of FPGA chips on the hardware platform for the LLRF system.

The configuration of the chips is done during consecutive stages. The configuration of the module *DATA&TIMING CONTROLLER* (Altera Cyclone 100K) is done in the first step. It is done by the active controller of the bus INTERNAL INTERFACE via the JTAG chain [10,11] or the bus PASSIVE SERIAL (ALTERA) [10].

After the activation, this module makes accessible four nondependent JTAG chains connected to the slots **A** - **D**. This solution enables full reconfiguration of JTAG chains in the internal structure of the FPGA matrix of the module *DATA & TIMING CONTROLLER*. The individual control is possible in each of the slots.

Broad usage of the JTAG standard is justified by its hardware implementation in all big FPGA matrices accessible on the market. The vendors offer also programming tools for the users in the "open source" form [10,11]. These tools are used to do own configurations of the system.

3.3. Distribution of fast synchronization signals

Distribution of fast synchronizing signals was divided into two groups: distribution of clock signals and distribution of triggering signals. The general configuration of the distribution network for synchronization signals between particular slots was presented in fig. 9.

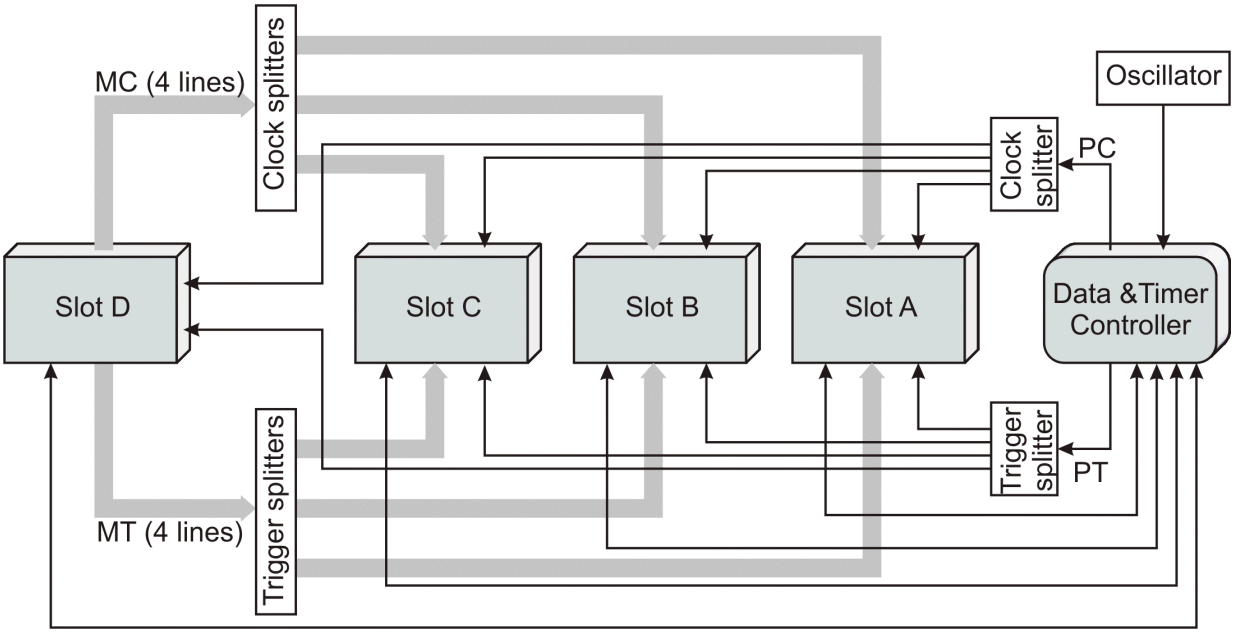

Fig. 9. Functional structure of fast synchronization signals for the LLRF system.

The central distribution module of fast synchronization signals is positioned in slot **D**. There were implemented four nondependent clock lines (*MC*) and trigger lines (*MT*). Each of these lines is separately multiplied to the slots **A** - **C**. This way provides electrical separation and impedance separation between the modules positioned in the slots.

The module *DATA & TIMING CONTROLLER* possesses the possibility to distribute a single global cock signal (*PC*) and trigger signal (*PT*). These signals are multiplied and electrically separated for the slots **A** - **D**. The local oscillator of 40MHz is connected to the modules to provide the autonomous work of the board. The autonomous work mode is used for servicing purposes. Each of the slots **A** - **D** is connected with the module *DATA & TIMING CONTROLLER* by a single duplex signal line of general purpose. This module may be used as a programmable re-distributor.

3.4. Distribution of fast data signals

The distribution of fast signals bases on 32 line point-to point buses. The connection wiring realized on the LLRF hardware platform does not contain the terminators. The complete interconnections between modules and slots are presented in fig. 10.

The configuration of fast data interconnections bus consists of three sections:

1. The signal buses *A-D* provide individual connections of the module *DATA & TIMING CONTROLLER* respectively with the slots **A** - **D**. The module may work in a hierarchical set up (centralized and acquisition) or as a data re-distributor. Using of the FPGA Cyclone to realize the module provides individual programming of the re-distribution network. The internal implementation of programmable reconfigurability of interconnections is possible.
2. The signal buses *DA*, *DB* and *DC* provide individual connections of the central slot **D** respectively with the slots **A** - **C**. The module may work in hierarchical set up (centralized, archiving) or as a re-distributor of data.

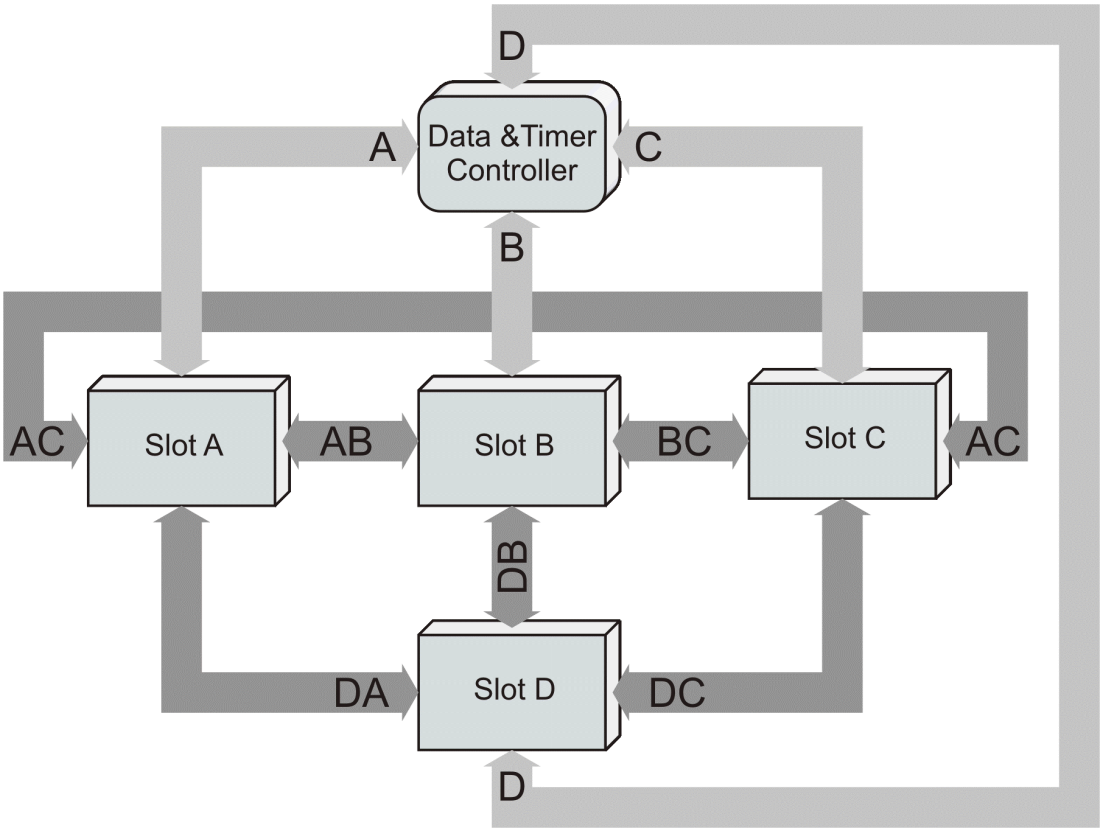

Fig. 10. Functional structure of all connections between hardware platform slots for the LLRF system.

3. The signal buses *AB* , *BC* and *AC* realize individual connections in a flat triangular set up. These are peer-to-peers connections respectively between the slots **A** - **C**. The buses provide, in this way, the fast data exchange between arbitrary slots and allow grouping of modules. The realization of individual hierarchical structures between the slots **A** – **C** is possible.

4. CONCLUSIONS

This paper synthetically describes the functional structure of the modular hardware platform for the LLRF control system. The platform is a universal, modular, reconfigurable backbone for specialized functional, FPGA based modules. The major idea of the system is presented. An advanced PCB was designed and practically realized in the 6HE size (EURO standard) for the LLRF control system. The common and repeating functionalities can be extracted from the LLRF system. It reduces the need to multiply some of the components in the functional modules. These components include: power supply for FPGA chips, communication with computer network, FPGA chip configuration, etc

All the technical details of the design were fit to the needs of the TESLA and X-FEL experiments requirements. The hardware platform has VME-BUS communication interface to co-operate with the DOOCS management and programming environment. A sub-system of fast clock and trigger signal distribution was realized.

The configuration of four user's slots provides realization of flat or hierarchical interconection network. The network realizes data transmission and synchronization. A big network flexibility configuration is embedded in this system, which can be tailored to the current needs.

There were performed and now are under tests two functional modules compatible with the hardware platform for the LLRF control system:

- Module for fast optical transmission. It contains duplex links for 2.4Gbps. The links are designed to concentrate the data flows.
- The control module for the LLRF system. It contains FPGA VirtexII V40000 chip with DSP blocks, 8 A/D channels and 4 D/A channels. It is designed to control the SC resonant cavities and the RF gun

5. ACKNOWLEDGEMENT

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