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A 81MHz IF Eight Channel Downconverter Board for a Digital RF Feedback System in TTF2

by

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Contents

Appendix

1. Introduction

Currently research in the development and verification of the fundamental constituents of matter and its interactions known as the Standard Model is conducted. It requires the design of high accuracy experimental instruments, which will enable us to obtain higher energy ranges as well as measuring instruments ensuring higher accuracy in evaluation of the measurands.
Estimation of parameters of the directly measurable signal on the basis of measured result of an other quantity, is an important extend factor of the range of measurability values in a given research area. It makes it possible to extend measurement efficiency as well as to increase the amount of source data that carry information about the phenomena processed.

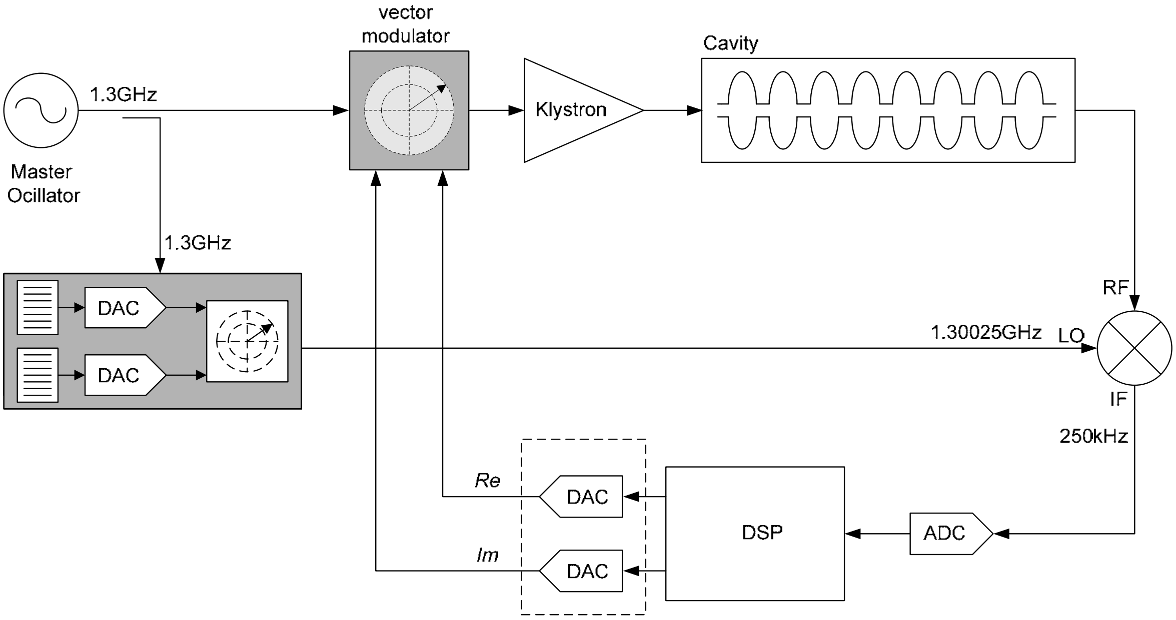

Figure 1. Block diagram of the Digital RF Feedback System.

The currently realized pilot project of new type linear accelerator - of TESLA Test Facility (TTF), one of goals of which is to realize the control vector sum for 32 cavities, with 1.3 ms pulsed power mode supplied by a single 10MW klystron for system of accelerating blocks. The target is to use to accelerate particles average accelerating gradient 25MV/m, which is at the same time the source of interference - mechanical deformations of the cavities. They are mainly caused by Lorenz force detuning and microphonics. The cavity deformations change the distribution of EM field, which causes the unwanted non-uniform particle acceleration, consequently resulting in energy dissipation. For compensation of the dynamical field distribution instability in each of the cavities, it requires the application of a stabilization system - RF feedback system (Fig.1).

The RF Feedback System (CS) is using to stabilize gradient and phase of the accelerating electromagnetic (EM) field in superconductivity cavity (SC) in TESLA Test Facility 2 (TTF2) and X-Ray Free Electron Laser (X-FEL). The requires target stabilization levels for the tested solution in the XFEL is respectively: $(\sigma_E /E)_{RMS} = 3\cdot 10^{-4}$ and $(\sigma\varphi)_{RMS} = 0.01°$, defined for 32 cavities. To meet of these requirements will result in higher efficiency of the acceleration process; therefore to obtain energy of the order of hundreds GeV, required luminosity has to be above $10^{33}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in order to achieve a reasonable event rate, and very small spot sizes at the collision point.

The control system corrects the EM field gradient and phase for the set of 32 accelerating modules on the basis of the field measurements take to advantage of downconverters, that are carried out on every end of the cavities. The EM field control accuracy in accelerating modules is mainly determined by measurement errors which are occurred during stabilization process, therefore it depends on the measurement process by the downconverter circuit which distribute signals carrying the information that is used to detect field parameters in a cavity, thus on the estimate of measurands.

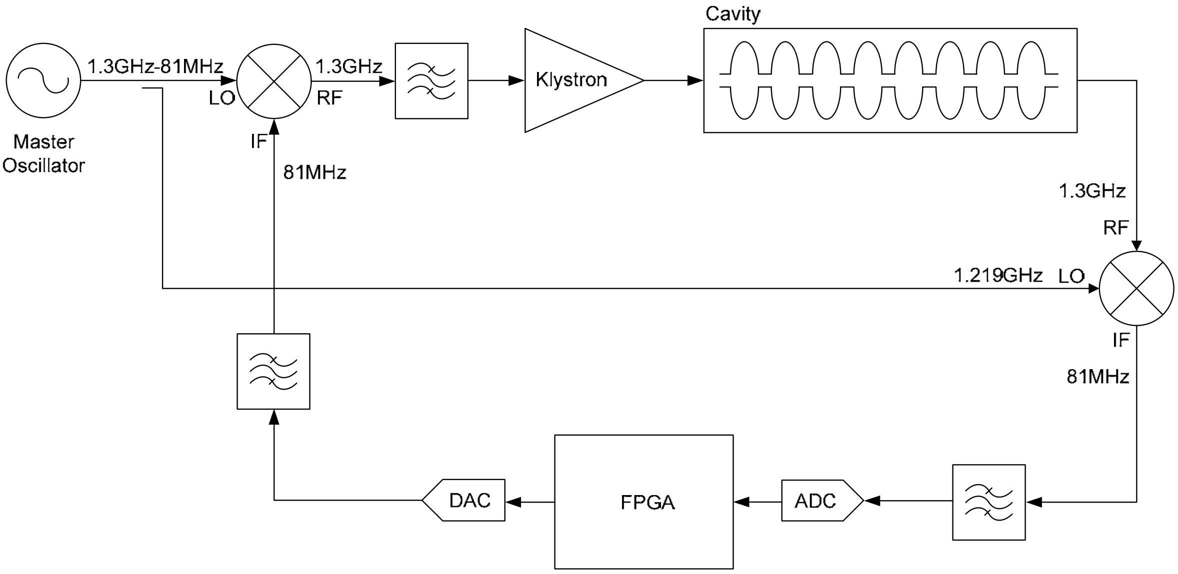

Figure 2. Block diagram of Digital RF Feedback System with IF 81MHz downconverter.

The present solution block diagram of the RF feedback system with IF_1 = 250kHz is shown in Fig.1. The downconverters convert the signals from individual cavities from 1.3GHz frequency to lower intermediate frequency (IF_1 =250kHz). The IF_1 frequency is located in the bandwidth of noise, which is generated in accelerator surroundings; therefore a new type of downconverter was designed and made with different intermediate frequency (IF_2 =81MHz), where modulation and demodulation is taken, in digital unit for EM field fluctuation detection, which will be implemented in FPGA (Fig.2.).

This frequency was also is changed because one of the new master oscillator's intermediate frequencies has the same output signal frequency. In addition, the solution using this value of *IF* can get lower relative jitter (for IF_1=250kHz ~ $0.4 \cdot 10^{-3}$%, for IF_2 = 81MHz ~ $1.23 \cdot 10^{-6}$ %). For the sake of gradient stability of the required order ~ 10^{-4}, it is necessary to use ADCs with $N < \log_2 10^4$ bit resolution, therefore $N > 14$ effective conversion bits. For required phase stability it is necessary to use a master oscillator which has a very low phase noise and very stable clock for ADC [1].

2. Requirement Specify

Necessary, to meet accuracy requirement of the (EM) field stabilization, at first new solution for design downconverter board (Fig.3) possessed of parameters respectively:

1. Input frequency 1.3GHz +/- 10MHz
2. Input impedance 50Ω
3. Input VSWR max. 1.5:1 desired, 1.8:1 acceptable
4. Nominal Input power range – 20dBm to + 3dBm
5. RF to LO and LO to RF isolation higher than 60dB
6. Intermediate frequency f_{IF} = 81MHz
7. Output bandwidth 20MHz
8. Output impedance 50Ω
9. Output VSWR max. 1.5:1 desired, 1.8:1 acceptable
10. Output level signal $v_{out} > 1V_{pp}$ at 1kΩ, at P_{RF} = -12dBm , P_{LO}=-10dBm
11. The1st to 2nd harmonic interval > 70dB
12. IIP3 > 15dBm, OIP3 > 20dBm
13. 1dB compression point: $P_{1dB,in}$ > 7 dBm
14. Inter-channel crosstalk > 60dB

3. Downconverter Board

The downconverter board consists of eight equal frequency conversion channels. The block diagram of the eight channel downconverter board is shown in Fig.3. The signals which are taken from cavities by the waveguide couplers are attenuated and distributed to individual downconverters channels. Attenuating of the signal has to assure optimal work condition of the mixers as regards linearity. The required linear range (for adequate harmonic level) for AD8343 mixers is for input power $P_{RF,in} \leq$. -12dBm.

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[1] This is the present consideration for RF feedback system.

Signal from master oscillator is distributed to downconverters through the splitter. The IF_2 signals (past frequency conversion) are gained by the amplification stage (which take to advantage of operational amplifier - AD8009) to get required downconverter output amplitude for further ADC's distribution. The component which is responsible for inter-channel crosstalk and isolation between individual channels on the PCB is distribution signal system.

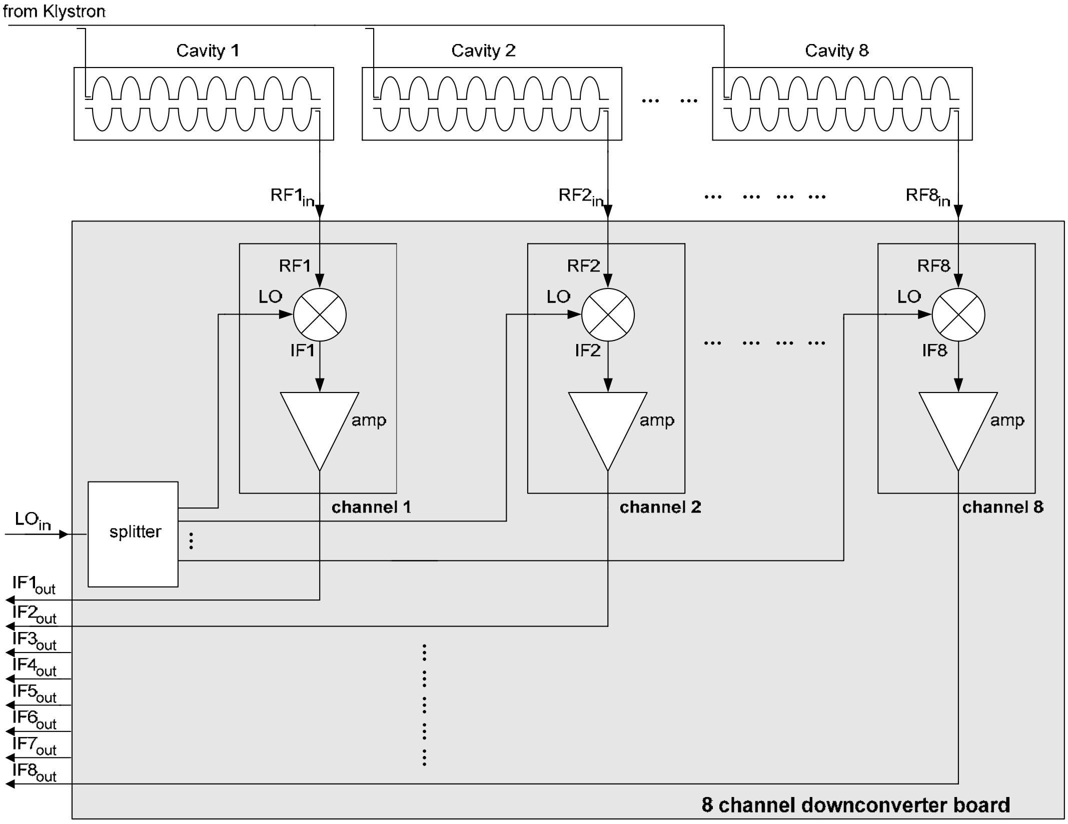

Figure 3. Block diagram of the eight channel downconverter board.

4. Downconverter Board - Circuit Solution

The downconverter circuit prototype has been realized with the use of active mixer AD8343 and AD8009 amplifier. The AD8343 is a high-performance broadband active mixer. Having wide bandwidth on all the ports and very low intermodulation distortion, the AD8343 is well suited for demanding transmit or receive channel applications. The AD8343 provides a typical conversion gain of 7.1dB. The integrated LO driver supports a 50Ω differential input impedance with low LO drive level, helping to minimize external component count. The schematic diagram for a single channel is shown in Fig.4. The prototypes of downconverters were realized on PCB DESY board LP. No. 7636-00, using the same mixer, this was used for IF_1 downconverter.

The AD8009 is an ultrahigh speed current feedback amplifier with a $5.500\,\mathrm{V}/\mu\mathrm{s}$ slew rate that results in a rise time of 545ps, making it ideal as a pulse amplifier. The high slew rate reduces the effect of slew rate limiting and results in the large signal bandwidth of 440MHz. The AD8009 is capable of delivering over 175mA of load current and will drive four back terminated video loads while maintaining low differential gain and phase error of 0.02% and 0.04° respectively. The high drive capability is also reflected in the ability to deliver 10dBm of output power at 70MHz with - 38dBc SFDR. Required frequency bandwidth of downconverter must be higher than:

$$B_{cavity} = \frac{f_0}{Q_{cavity}} = \frac{1.3\cdot 10^9}{3\cdot 10^6} = 433{,}33 Hz \tag{4.1}$$

where:

$$Q_{cavity} = \frac{f_0}{2\Delta f} = \frac{f_0}{f_u - f_d} \tag{4.2}$$

A main task of the project was to design the matching circuit, which would match the mixer to the amplifier for 81MHz, and to design the amplifier, which would give 2 V_{PP} in the output. The output impedance of the mixer is 359,5 – 778,95i Ω and input impedance of amplifier (Fig.4) is 326.57 - 36,77 Ωi Ω, at 81MHz. For the source which has impedance $Z_o = R_o + j\,X_o$, and $Z_L = R_L + j\,X_L$ load, and assume $R_0 > 0$, $R_L > 0$. The load to source is matched when $P = P_{\max}$. The current for is:

$$I = \frac{E}{Z_o + Z_L} = \frac{E}{(R_o + R_L) + j(X_o + X_L)} \tag{4.3}$$

The power on the load is:

$$P = \frac{1}{2}|I|^2 R = \frac{|E|^2 R}{2[(R_o + R_L)^2 + (X_o + X_L)^2]} \tag{4.4}$$

therefore:

$$P_L = P_{\max} \Leftrightarrow R_L = R_o, X_L = X_o \quad or \quad Z_L = Z_o^* \tag{4.5}$$

The gain of amplifiers AD8009 for to meet of condition:

$$R11 = R12 \text{ i } R21 = R22 \tag{4.6}$$

is given by:

$$k_u = \frac{R21}{R11} = \frac{R22}{R12} \tag{4.7}$$

$$v_{out} = \frac{R21}{R11}(v_2 - v_1) = \frac{R22}{R12}(v_2 - v_1) \tag{4.8}$$

The matched output impedance of mixer is 416,59+52,21i Ω, where input impedance of amplifier is 326.57 - 36,77 Ω. The mixer output impedance and amplifier input impedance on Smith chart is shown in Fig.5. The Schematic diagram of one single channel of downconverter is presented in Fig4. For this matching circuit solution the reflection coefficient is $\Gamma_{amp,mix} = 0{,}12$.

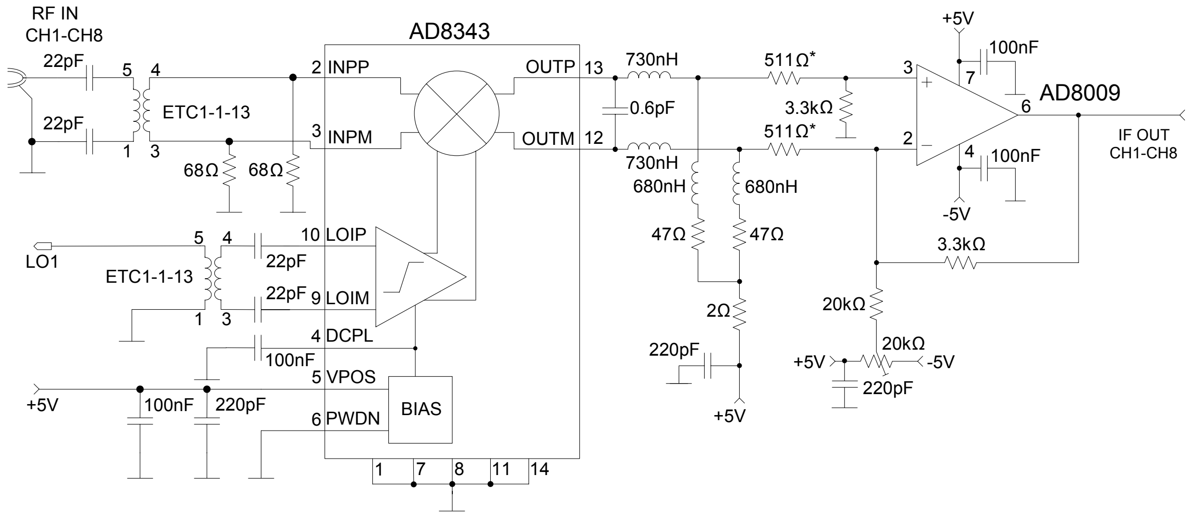

Figure 4. Schematic diagram of the single channel downconverters board.

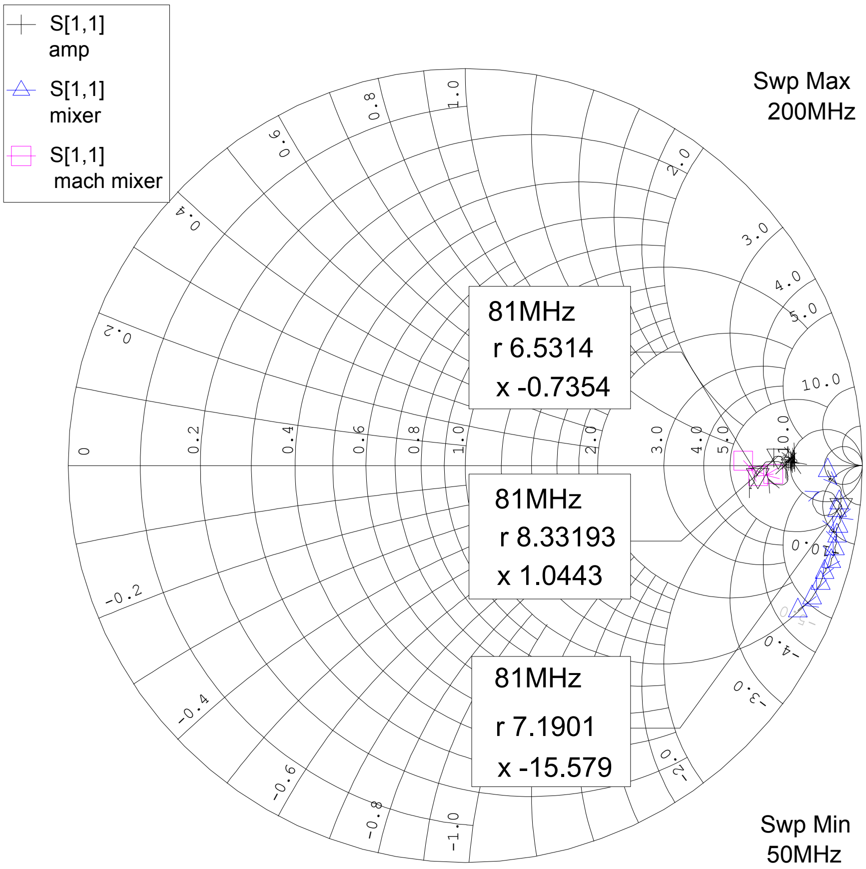

Figure 5. The impedances, mixer output and amplifier input.

5. Measurements Results

The measurements were done for tests realized circuits, as well as for tuning and performance optimization purposes. The following parameters for all channels of the downconverter board were determined:

- Output power for first, second and third harmonic vs. input power
- 1st to 2nd harmonic interval
- 1dB compression point

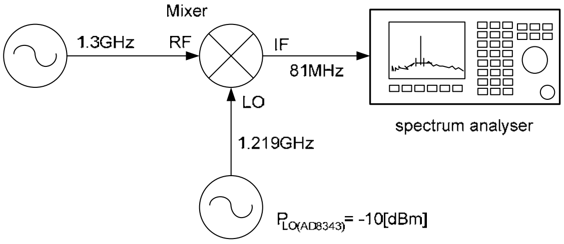

Figure 5. Measuring setup for measurements of: output power for 1st, 2nd and 3rd harmonic vs. input power, at P_{LO} is constant, 1st to 2nd harmonic interval, 1dB compression point.

- Third-order intermodulation

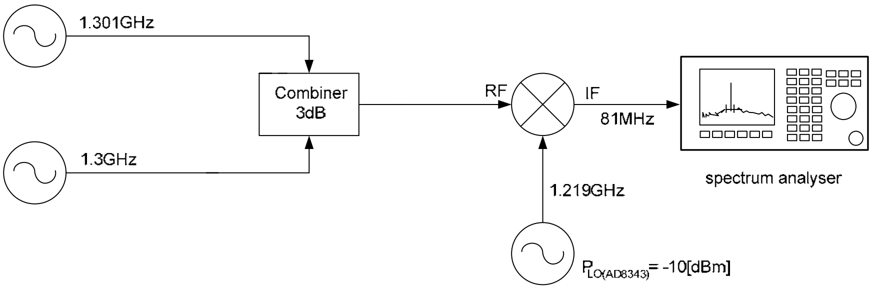

Figure 6. Measuring setup for measurements of third-order intermodulation.

- Inter-channel crosstalk
- Isolation

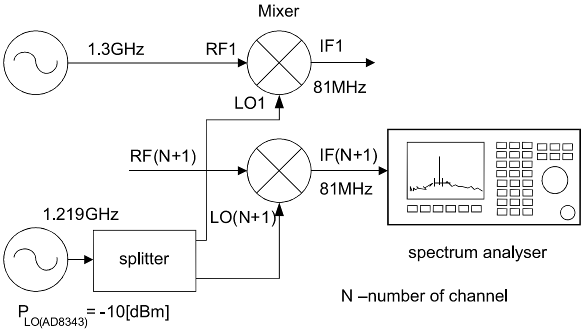

Figure.7. Measuring setup for measurements of inter-channel crosstalk and isolation.

Table 1. The 1st harmonic level, at $P_{LO,in}$ = 0dBm, $f_{LO,in}$ = 1,219GHz, $f_{RF,in}$= 1,3GHz.

$P_{RF,in}$	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	ideal
[dBm]	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**
-30	-24,54	-24,28	-24,17	-24,46	-24,49	-24,38	-24,21	-24,59	-24,39
-27	-20,9	-21,2	-21,02	-21,29	-21,35	-21,16	-21,08	-21,48	-21,18
-24	-17,95	-18,26	-18,1	-18,37	-18,42	-18,22	-18,17	-18,54	-18,25
-21	-14,94	-15,22	-15,01	-15,26	-15,36	-15,18	-15,1	-15,49	-15,19
-18	-11,92	-12,23	-12,07	-12,31	-12,4	-12,19	-12,12	-12,51	-12,21
-15	-9,01	-9,32	-9,13	-9,55	-9,48	-9,28	-9,22	-9,66	-9,33
-12	-6,38	-6,36	-6,31	-6,35	-6,38	-6,4	-6,39	-6,41	-6,23
-6	-4,09	-4,25	-4,25	-4,25	-4,24	-4,21	-4,17	-4,18	-3,22
-9	-1,3	-1,6	-1,56	-1,7	-1,51	-1,51	-1,44	-1,33	-0,21
-3	2,86	2,5	2,69	2,45	2,42	2,53	2,59	2,28	2,79
0	5,97	5,41	5,55	5,29	5,23	5,4	5,46	5,14	5,79

Table 2. The 2nd harmonic level, at $P_{LO,in}$ = 0dBm, $f_{LO,in}$ = 1,219GHz, $f_{RF,in}$= 1,3GHz.

$P_{RF,in}$	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	ideal
[dBm]	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**
-30	-95,4	-98	-97,54	-98,14	-101,93	-97,23	-99,43	-103,6	-100
-27	-91,21	-95,35	-93,76	-94,63	-97,12	-93,13	-94,32	-95,65	-94,8
-24	-85,53	-90,09	-87,15	-89,36	-93,95	-88,16	-90,23	-93,8	-89,6
-21	-79,64	-84,31	-82,24	-79,15	-87,14	-82,02	-84,56	-88,62	-83,9
-18	-74,02	-78,42	-75,43	-76,94	-81,98	-76,3	-77,66	-81,92	-78,4
-15	-74,5	-72,49	-70,43	-76,53	-72,11	-71,37	-73,63	-71,5	-72,94
-12	-66,5	-66,6	-64,42	-65,02	-70,29	-65,92	-67,25	-68,7	-67,63
-6	-63,5	-62,62	-59,14	-63,9	-58,42	-59,77	-60,57	-59,9	-62,32
-9	-50,47	-53,9	-53,09	-51,82	-57,6	-52,93	-56	-57,68	-57,02
-3	-47,03	-48,82	-47,85	-47,3	-52	-46,67	-49,4	-53,44	-51,71
0	-42,27	-41,08	-40,03	-40,07	-43,5	-38,7	-44,51	-43,75	-46,40

Table 3. The 3rd harmonic level, at $P_{LO,in}$ = 0dBm, $f_{LO,in}$ = 1,219GHz, $f_{RF,in}$= 1,3GHz.

$P_{RF,in}$	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	ideal
[dBm]	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**
-30	-127,91	-128,29	-128,73	-127,37	-128,29	-127,95	-129,68	-128,84	-128,38
-27	-119,02	-119,20	-119,66	-118,41	-119,31	-118,78	-120,54	-119,84	-119,34
-24	-110,14	-110,108	-110,59	-109,44	-110,33	-109,61	-111,4	-110,84	-110,31
-21	-101,58	-100,74	-100,78	-100,18	-100,77	-100,44	-101,33	-101,28	-100,88
-18	-92,68	-92,59	-93,16	-92,03	-92,75	-91,8	-94,3	-93,63	-92,86
-15	-83,47	-83	-83,72	-83,06	-84,14	-81,93	-83,95	-84,46	-83,46
-12	-74,06	-73,34	-74,11	-73,16	-74,22	-72,52	-74,6	-74,33	-73,79
-6	-65,27	-64,52	-65,35	-64,38	-65,39	-63,7	-65,83	-65,5	-64,99
-9	-56,57	-55,25	-56,42	-55,1	-56,23	-54,51	-56,83	-56,52	-55,93
-3	-47,62	-46,17	-46,55	-46,46	-47,14	-44,98	-46,82	-47,67	-46,67
0	-39,91	-37,95	-38,21	-38,38	-38,84	-36,85	-38,43	-39,35	-38,49

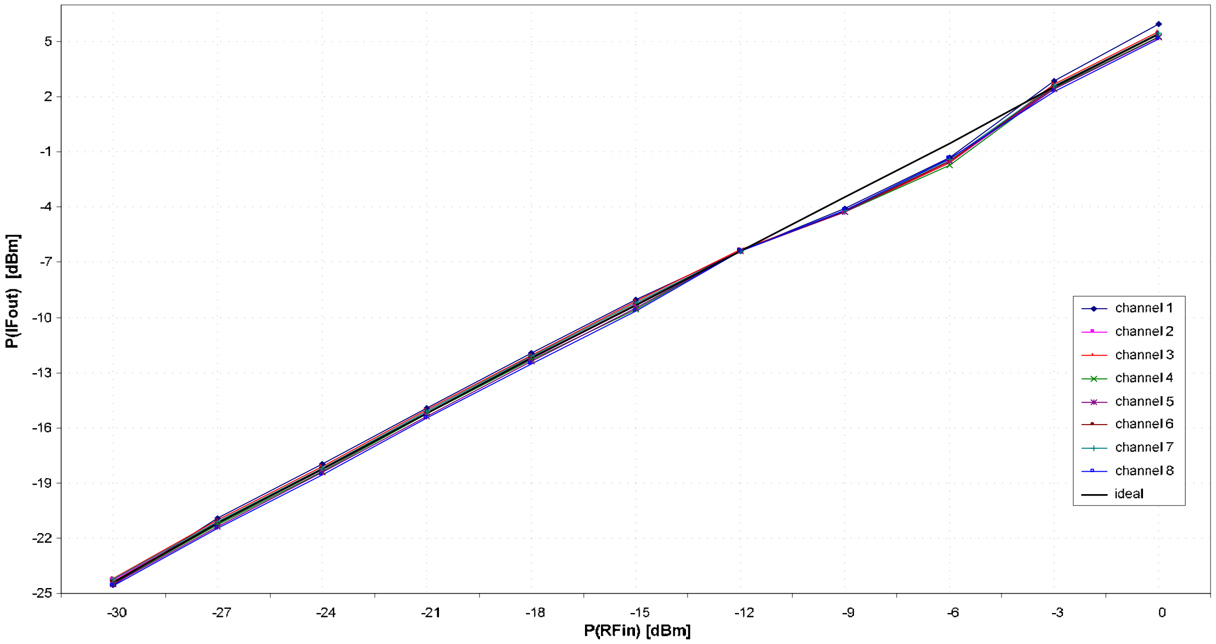

Figure 8. The 1st harmonic output level vs. input power.

Output power vs. input power for 1st harmonic for all channels on downconverter board is shown in Fig.8, where local oscillator power is constant. The high linearity is ± 0,18dB for $P_{RFin} \leq 12$dBm. Maximum scatter of output signal level results is ± 0,37dB.

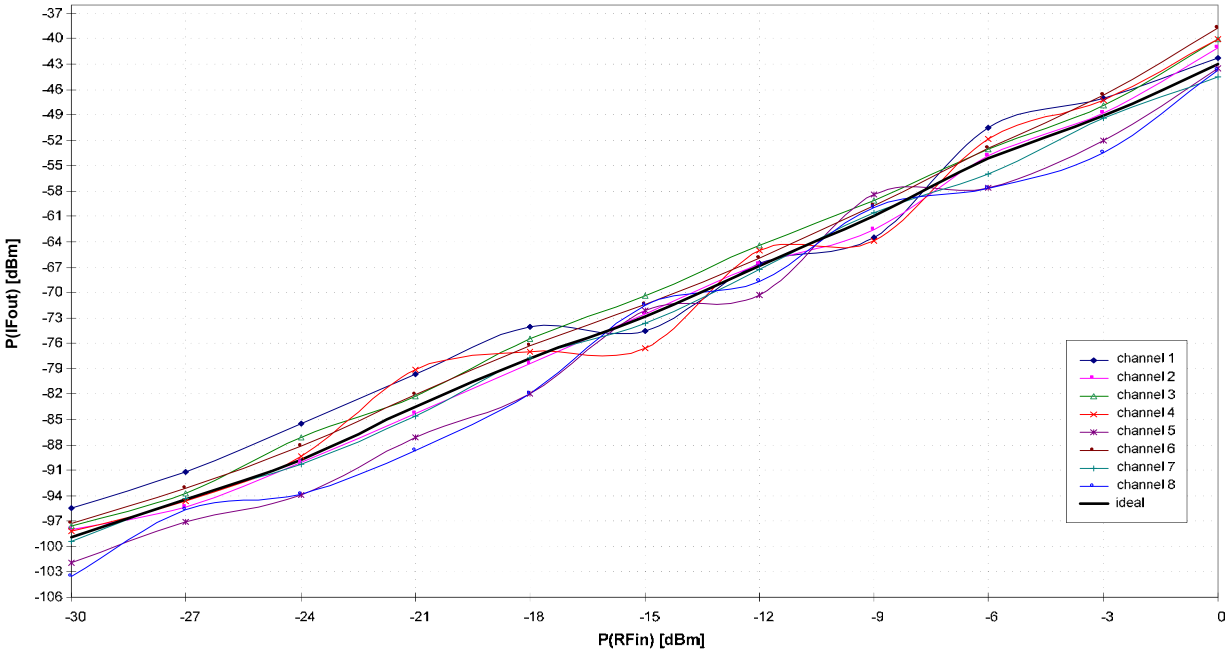

Figure 9. The 2nd harmonic output power level vs. input power.

Output power vs. input power for 2nd harmonic for all channels on downconverter board is shown in Fig.9, where local oscillator power is constant. The high linearity is ± 2,1dB for $P_{RFin} \leq$ -12dB. The maximum scatter of output signal level results is ± 3,2dB. The downconverter introduces even harmonics distortion, that in this application, at the quadrature stimulation, does not influence the parameters of the conversion line.

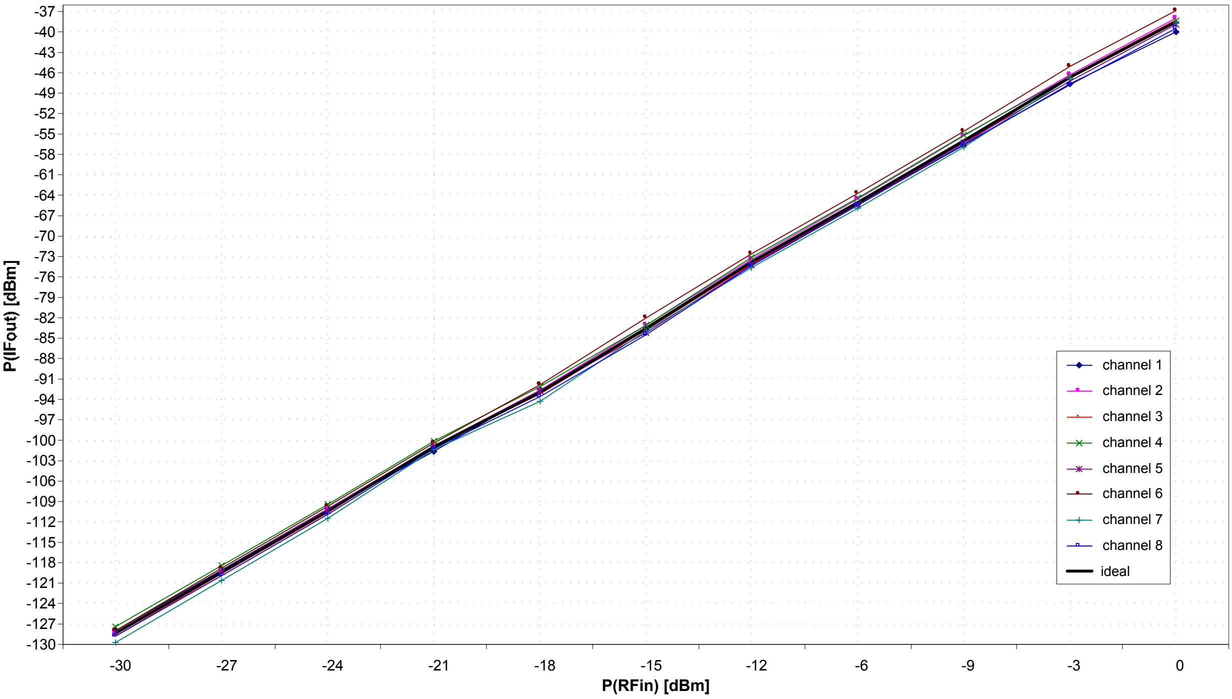

Figure 10. The 3rd harmonic output power level vs. input power.

Output power vs. input power for 3rd harmonic for all channels on downconverter board is shown in Fig.10, where local oscillator power is constant. The high linearity is ± 1,3dB for $P_{RFin} \leq$ 12dBm. The maximum scatter of the output signal level is ± 1,7dB.

Table 2. The 1st to 2nd harmonic interval.

PLO,in = 0dBm, fLO,in = 1,219GHz, fRF,in = 1,3GHz								
1st to 2nd harmonic interval								
$P_{RF,in}$	**Channel 1**	**Channel 2**	**Channel 3**	**Channel 4**	**Channel 5**	**Channel 6**	**Channel 7**	**Channel 8**
[dBm]	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**
-30	70,86	73,72	73,37	73,68	77,44	72,85	75,22	79,01
-27	70,31	74,15	72,74	73,34	75,77	71,97	73,24	74,17
-24	67,58	71,83	69,05	70,99	75,53	69,94	72,06	75,26
-21	64,7	69,09	67,23	63,89	71,78	66,84	69,46	73,13
-18	62,1	66,19	63,36	64,63	69,58	64,11	65,54	69,41
-15	65,49	63,17	61,3	66,98	62,63	62,09	64,41	61,84
-12	60,12	60,24	58,11	58,67	63,91	59,52	60,86	62,29
-6	59,41	58,37	54,89	59,65	54,18	55,56	56,4	55,72
-9	49,17	52,3	51,53	50,12	56,09	51,42	54,6	56,35
-3	49,89	51,32	50,54	49,75	54,42	49,2	51,99	55,72
0	48,24	46,49	45,58	45,36	48,73	44,1	49,97	48,89

Table 3. The 1dB compression point

PLO,in = 0dBm, fLO,in = 1,219GHz, fRF,in = 1,3GHz								
1dB compression point								
$P_{RF,in}$	**Channel 1**	**Channel 2**	**Channel 3**	**Channel 4**	**Channel 5**	**Channel 6**	**Channel 7**	**Channel 8**
[dBm]	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**
-30	-23,24	-23,3	-23,75	-23,51	-23,75	-23,6	-23,45	-23,83
-27	-20,44	-20,37	-20,9	-20,46	-20,46	-20,6	-20,63	-20,97
-24	-17,36	-17,32	-17,86	-17,42	-17,8	-17,56	-17,36	-17,92
-21	-14,4	-14,3	-14,88	-14,47	-14,84	-14,6	-14,61	-14,95
-18	-11,28	-11,26	-11,77	-11,44	-11,75	-11,54	-11,5	-11,88
-15	-8,34	-8,3	-8,81	-8,48	-8,79	-8,56	-8,52	-8,88
-12	-5,3	-5,28	-5,76	-5,48	-5,75	-5,55	-5,52	-5,86
-9	-2,41	-2,34	-2,83	-2,43	-2,83	-2,6	-2,62	-2,92
-6	0,53	0,62	0,1	0,43	0,11	0,35	0,32	0,01
-3	3,5	3,63	3,08	3,48	3,12	3,38	3,34	3,01
0	6,42	6,52	6,1	6,42	6,03	6,31	6,28	5,95

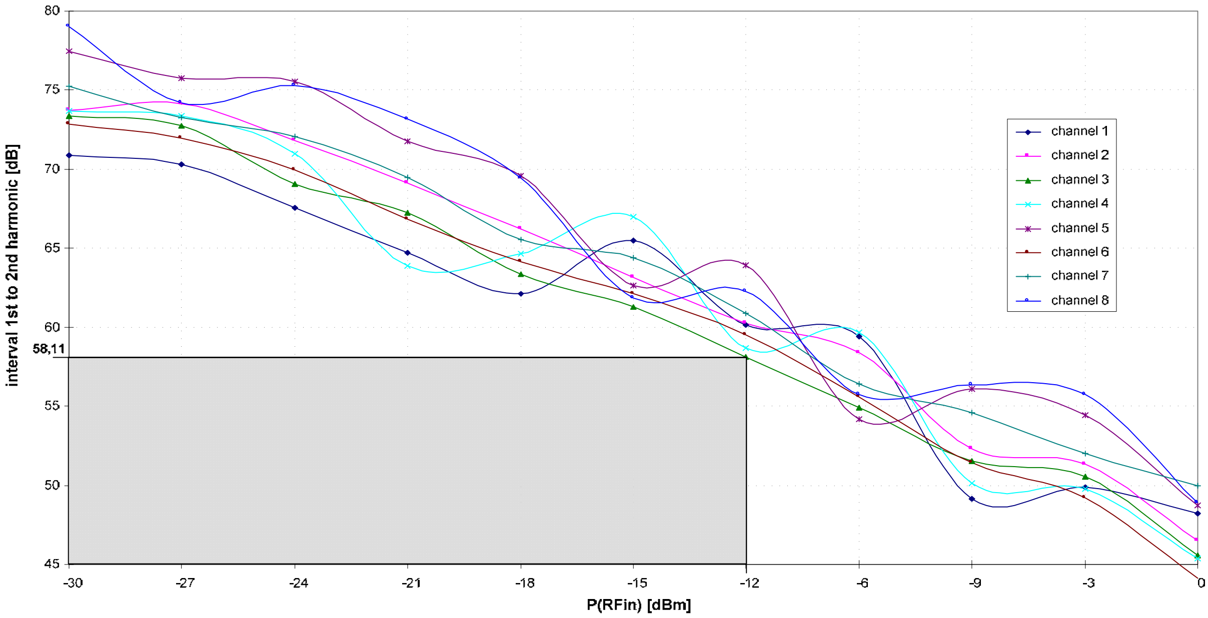

Figure 11. The 1st to 2nd harmonic interval.

A 1st to 2nd harmonic interval for all channels of downconverter board is shown in Fig.11. The lowest 1st to 2nd harmonic interval is for 3rd channel (1st to 2nd harmonic interval = 58,11dB for $P_{RFin} \leq$ -12dBm. In the (foregoing) above figure, the range of downconverter's linear work for P_{RF} have been marked

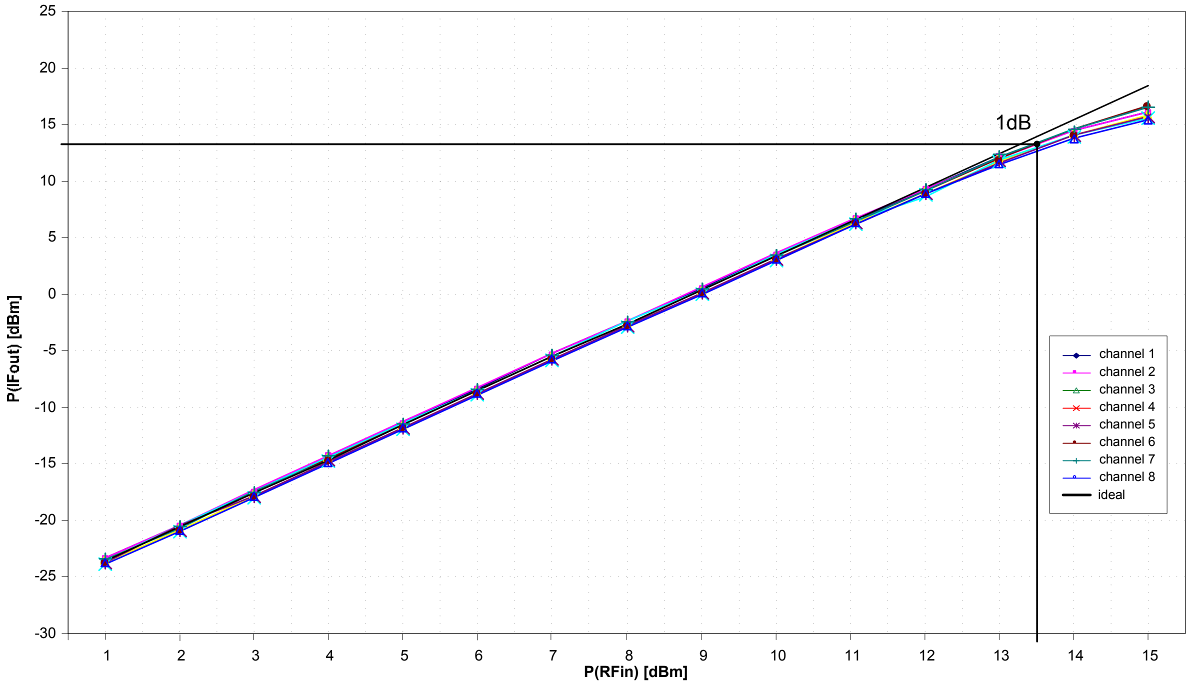

Figure 12. The 1dB compression point.

The 1dB compression point (average input *1dB* is 13,5dBm) is shown in Fig.12, that to make possible high level signal output without the harmonic distortion.

Third-order intermodulation measurements

Table 4. Third-order intermodulation channel 1st & 2nd

	channel 1			channel 2		
P(IF)out	**1st harm**	**IM3-**	**IM3+**	**1st harm**	**IM3-**	**IM3+**
[dBm]	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**
-21	-15,02	-82,01	-85,9	-15,54	-85,54	-84,91
-18	-11,51	-77,23	-77,58	-11,51	-79,17	-79,62
-15	-8,47	-67,08	-68,22	-9,53	-72,15	-71,38
-12	-5,56	-59,21	-59,08	-6,47	-61,86	-62,44
-9	-3,59	-54,19	-53,65	-3,57	-54,23	-54,32
-6	-0,23	-43,09	-43,16	-0,66	-45,69	-45,36
-3	2,45	-35,29	-36,36	2,14	-37,82	-37,68
0	5,3	-28,03	-29,43	4,74	-30,68	-30,58
3	7,84	-21,58	-22,25	7,73	-22,8	-22,28
6	9,98	-13,16	-13,31	9,77	-12,77	-10,98
9	11,71	-6,92	-4,89	11,21	-6,43	-4,48

Table 5. Third-order intermodulation channel 3rd & 4th

	channel 3			channel 4		
P(IF)out	**1st harm**	**IM3-**	**IM3+**	**1st harm**	**IM3-**	**IM3+**
[dBm]	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**
-21	-16,22	-85,33	-87,1	-14,52	-84,09	-86,85
-18	-13,28	-82,12	-81,2	-12,89	-78,37	-77,88
-15	-10,26	-73,28	-73,9	-8,6	-69,35	-68,29
-12	-7,2	-64,61	-66,4	-6,81	-59,35	-63,49
-9	-4,45	-56,53	-57,3	-4,45	-55,58	-56,79
-6	-1,4	-47,5	-48,3	-1,57	-46,6	-48,5
-3	1,55	-38,94	-39,6	1,21	-40,13	-40,78
0	4,37	-32,1	-31,5	4,59	-29,19	-29,62
3	6,98	-24,33	-23,8	7,31	-19,09	-18,95
6	9,12	-15,06	-14,3	9,12	-10,72	-9,32
9	10,65	-8,51	-6,84	10,22	-6,01	-5,01

Table 6. Third-order intermodulation channel 5th & 6th

	channel 5			channel 6		
P(IF)out	**1st harm**	**IM3-**	**IM3+**	**1st harm**	**IM3-**	**IM3+**
[dBm]	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**
-21	-16,72	-85,83	-86,57	-15,33	-84,94	-87,14
-18	-13,05	-78,47	-78,4	-11,7	-78,64	-82,62
-15	-9,96	-70,13	-72,3	-10,44	-70,93	-71,25
-12	-7,87	-64,3	-61,48	-7,34	-61,58	-62,86
-9	-4,62	-52,7	-53,66	-2,45	-57,91	-53,96
-6	-0,85	-45,73	-46,49	-0,72	-47,8	-47,87
-3	1,47	-37,6	-36,83	2,07	-39,24	-39,99
0	4,12	-30,09	-31,06	4,85	-31,98	-32,74
3	6,78	-22,49	-23,21	7,88	-25,26	-24,74
6	8,84	-12,56	-12,89	10,3	-17,25	-15,8
9	10,54	-6,54	-5,57	12,1	-8,63	-5,25

Table 7. Third-order intermodulation channel 7th & 8th

	channel 7			channel 8		
P(IF)out	**1st harm**	**IM3-**	**IM3+**	**1st harm**	**IM3-**	**IM3+**
[dBm]	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**
-21	-14,9	-84,37	-87,88	-15,09	-87,23	-86,4
-18	-11,88	-79,93	-79,37	-12,91	-80,01	-79,24
-15	-9,01	-71,57	-71,67	-10,07	-70,74	-70,9
-12	-5,94	-61,83	-63,37	-7,68	-62,2	-63,6
-9	-3,09	-53,13	-54,84	-4,6	-55,8	-56,1
-6	0,31	-45,56	-46,32	-1,71	-46,8	-47,2
-3	2,62	-36,94	-38,18	1,13	-39,6	-38,6
0	5,38	-29,95	-31,38	4,96	-28,95	-29,74
3	7,88	-24,55	-24,54	7,8	-20,75	-21,34
6	10,25	-15,79	-14,84	9,97	-11,19	-10,31
9	11,98	-8,16	-5,86	10,67	-7,17	-4,7

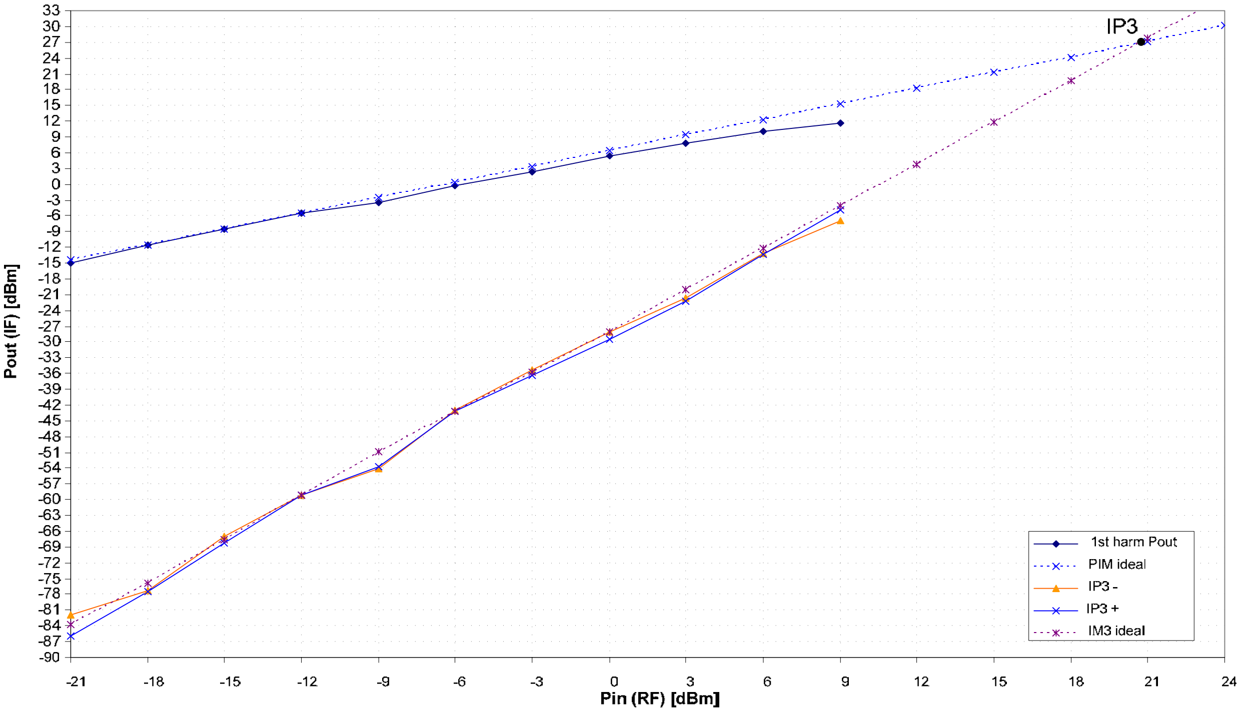

Figure 13. The 1st channel third-order intermodulation.

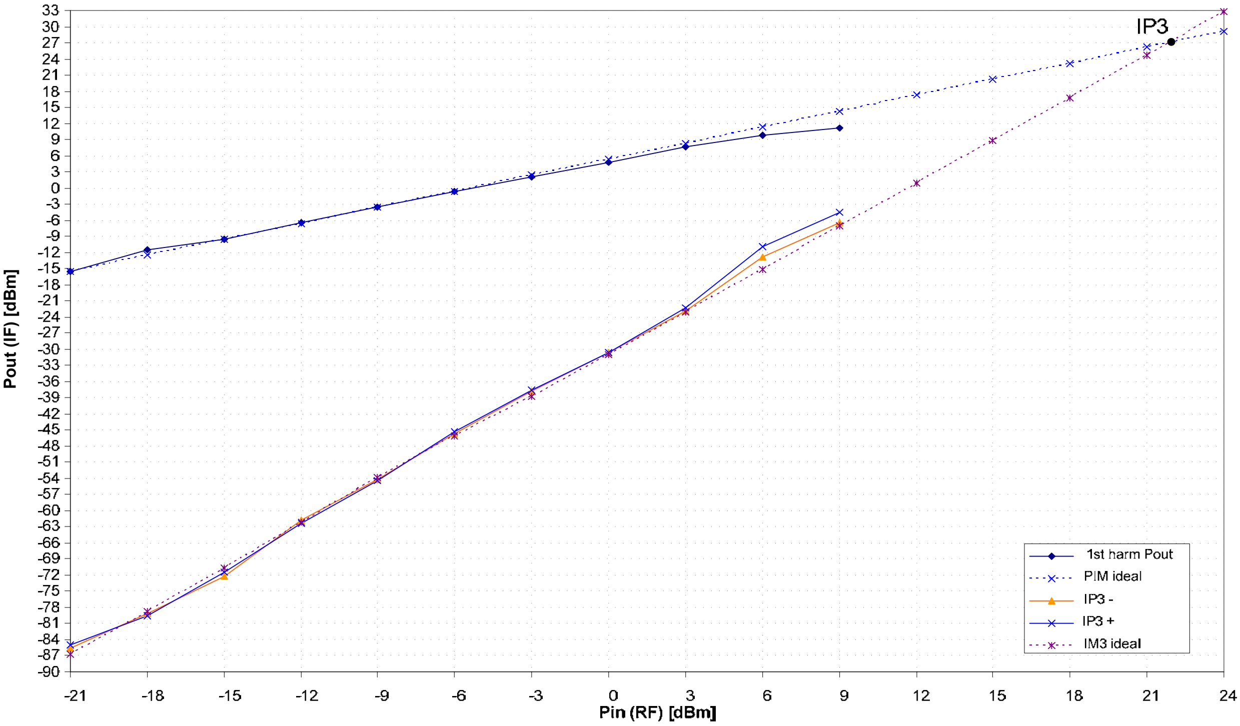

Figure 14. The 2nd channel third-order intermodulation.

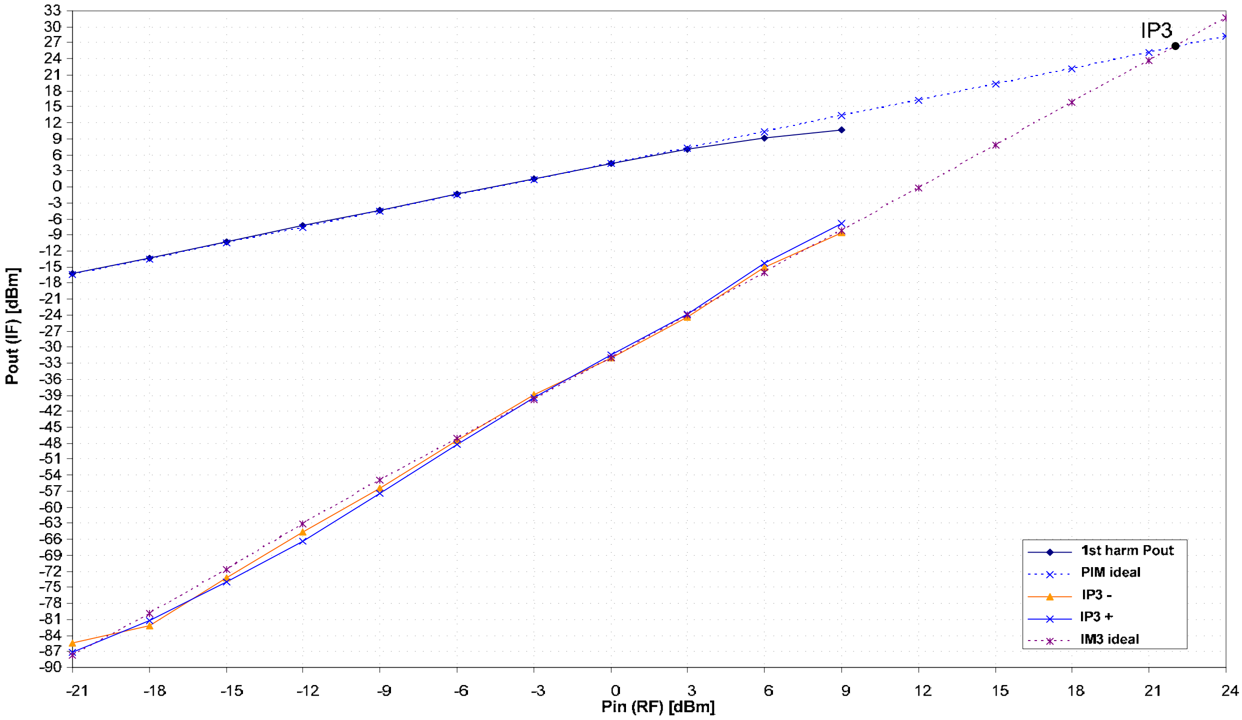

Figure 15. The 3rd channel third-order intermodulation.

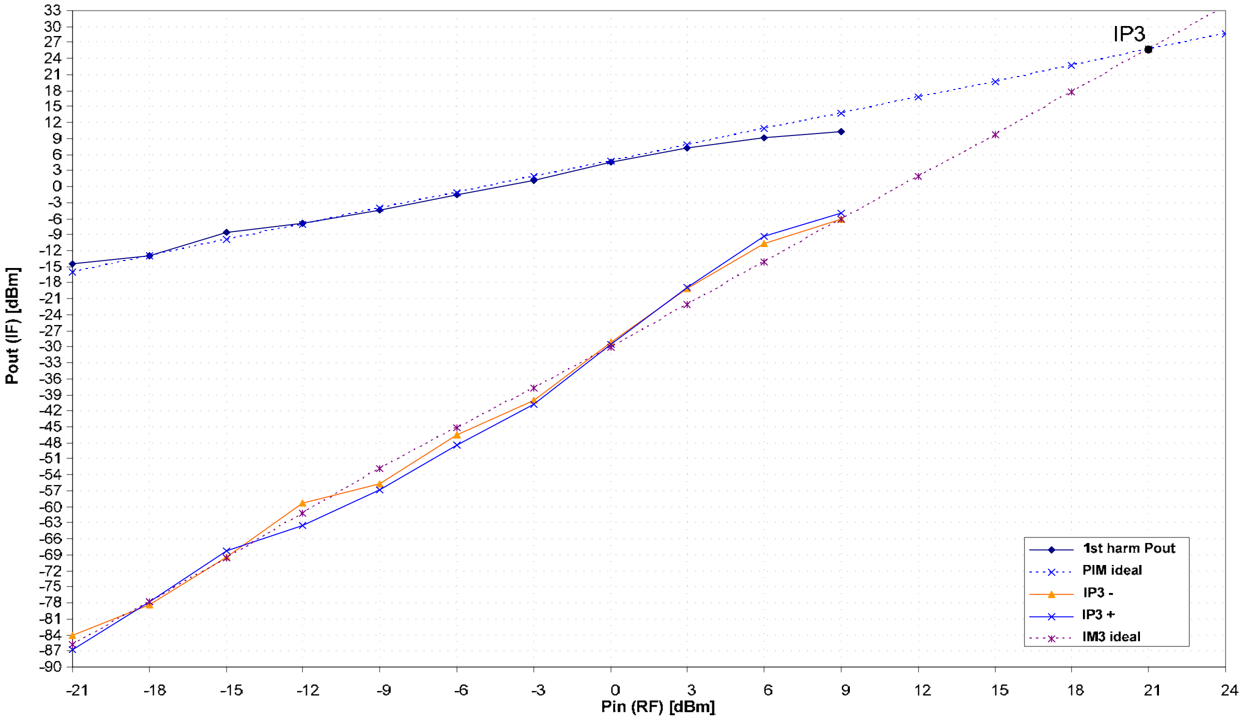

Figure 16. The 4th channel third-order intermodulation.

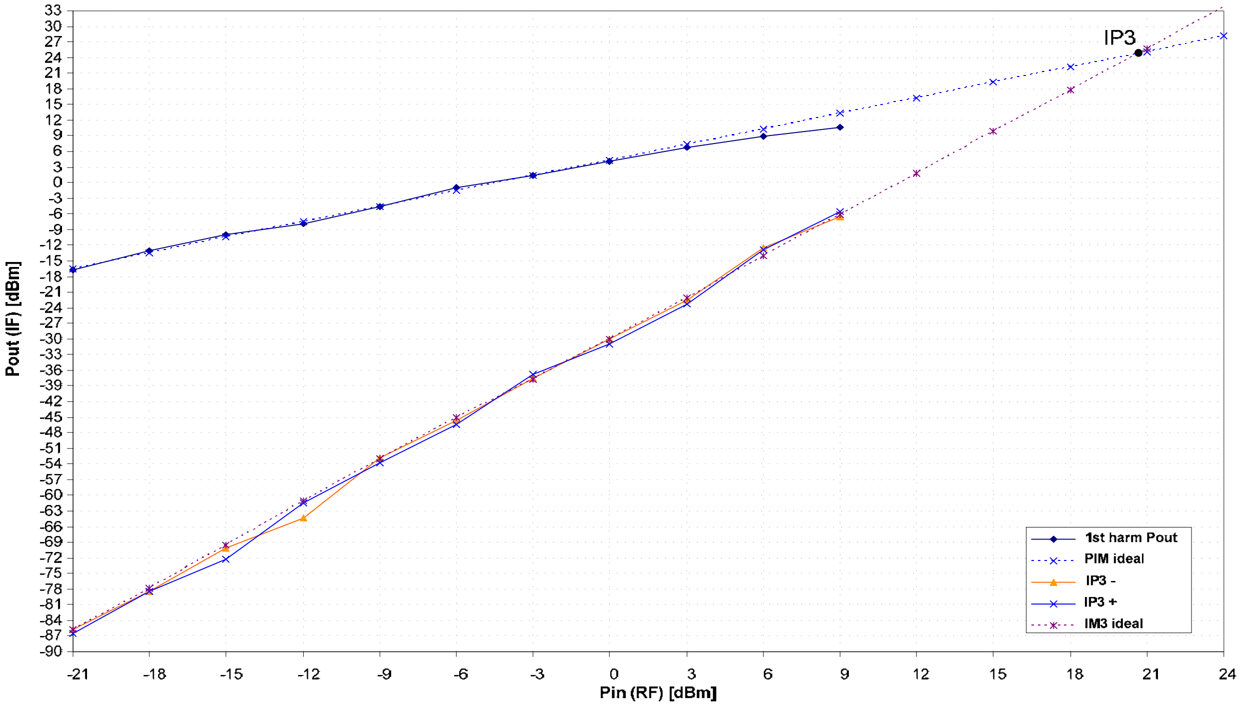

Figure 17. The 5th channel third-order intermodulation.

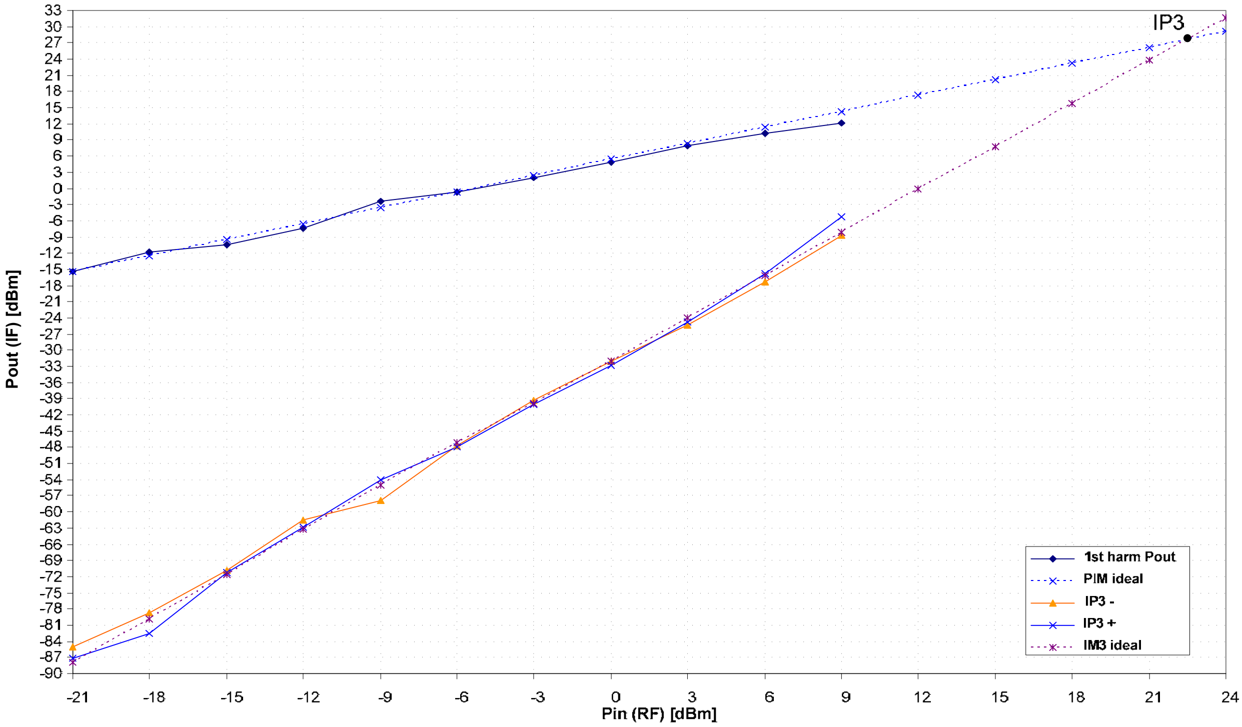

Figure 18. The 6th channel third-order intermodulation.

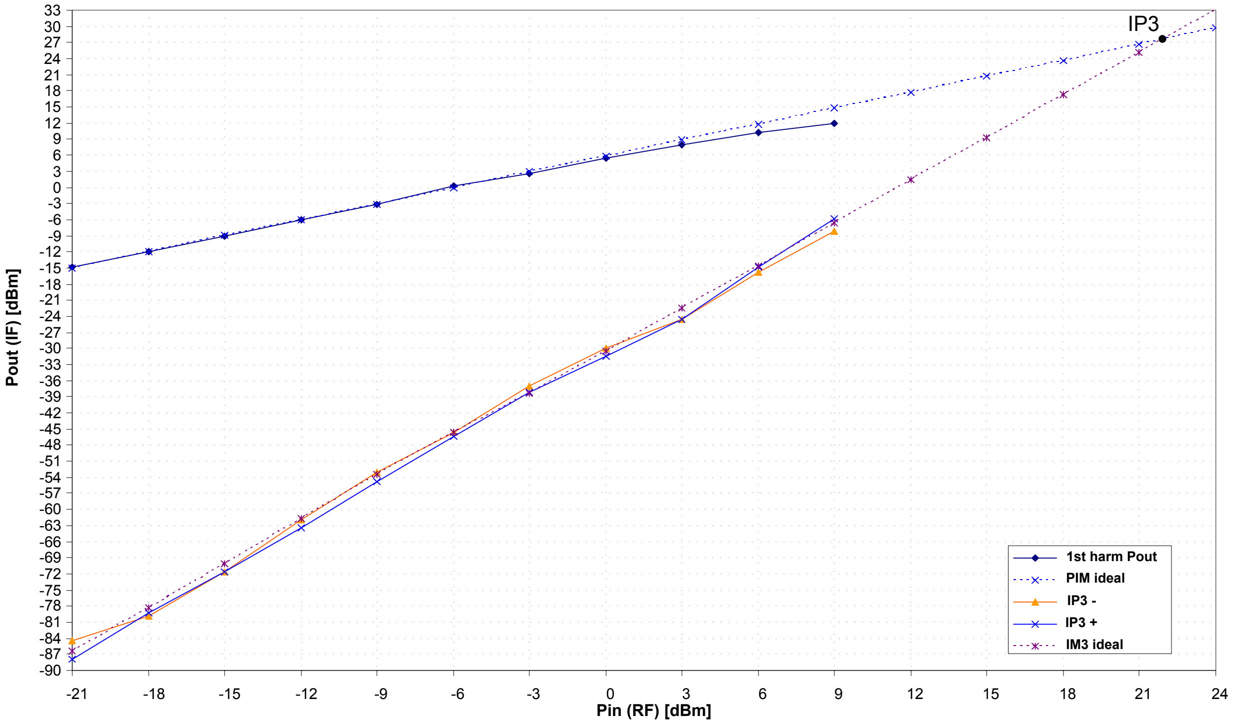

Figure 19. The 7th channel third-order intermodulation.

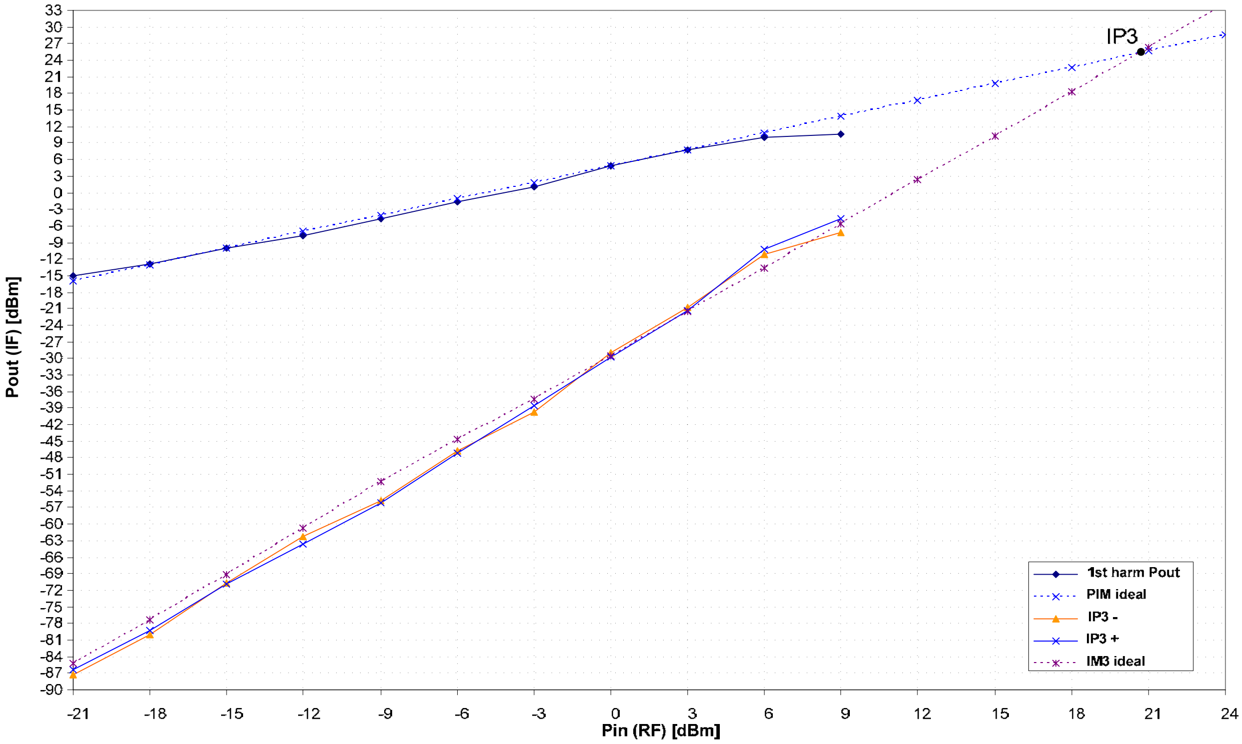

Figure 20. The 8th channel third-order intermodulation.

In Figures 13 - 20 third-order intermodulation characteristics for all channels of the downconverter board are shown. The number values for *IP3* and *1dB* compression point is shown in 8th Table. The minimum IP3 is 21dBm (Pin) and 26,5dBm (Pout) for 8th channel.

Table 8. IP3 & 1dB summary

			channel 1	**channel 2**	**channel 3**	**channel 4**	**channel 5**	**channel 6**	**channel 7**	**channel 8**
IP3	**Pin**	**[dBm]**	21	22	23,5	21	20,5	22,5	22	21
	Pout	**[dBm]**	27	27	26	26	25,5	25	27	26,5
1dB	**Pin**	**[dBm]**	7,5	7,55	7,6	7,65	7,7	7,75	7,78	8
	Pout	**[dBm]**	13	13,1	13,2	13,2	13,3	13,3	13,4	13,5

Table.9. Inter-channel crosstalk (P$_{(RF)in}$=-12dBm P$_{(LO)in}$=0dBm)

	channel	**channel**	**channel**	**channel**	**channel**	**channel**	**channel**	**channel**
channel	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
	[dBm]	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**	**[dBm]**
1		58,03	60,95	62,54	65,93	69,11	66,66	66
2	55,26		58,87	59,96	64,48	65,86	67,36	65,96
3	52,09	55,23		61,28	62,81	65,87	65,09	66,38
4	51,75	53,38	64,05		58,69	64,39	64,22	64,97
5	51,57	52,91	56,24	62,05		64,27	63,52	66,31
6	51,01	52,85	56,34	57,57	67,54		61,6	64,24
7	50,84	52,91	56,83	58,3	63,07	63,91		63,1
8	51,25	52,93	55,75	56,36	60,06	62,73	59,65	

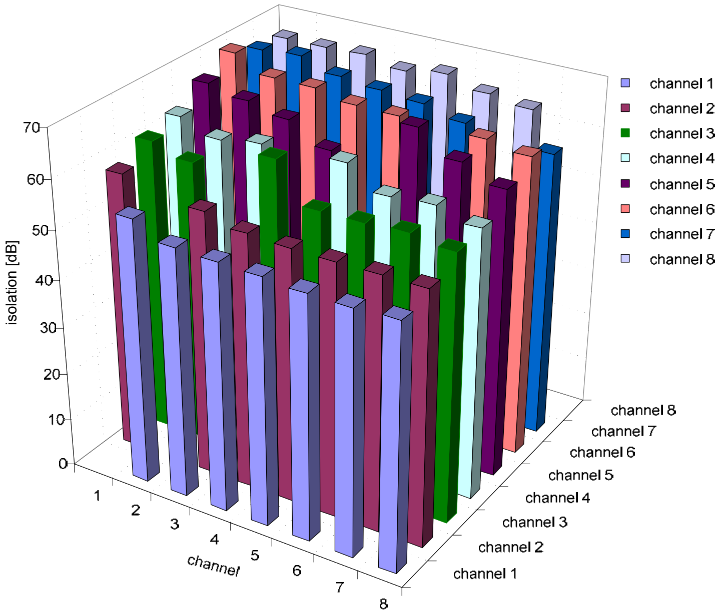

Figure 21. The inter-channel crosstalk.

Figure 21 and in Table 9th show inter-channel crosstalk. The minimum value of inter-channel crosstalk is for 1st channel (51dB). That is connected with structure of microstrip line for 1st channel. That solution meets the input requirements.

Table 10. Isolation

	IF to LO	**IF to RF**	**RF to IF**	**RF to LO**	**LO to IF**
channel	**[dB]**	**[dB]**	**[dB]**	**[dB]**	**[dB]**
1	101,69	63,51	75,26	81,86	63,72
2	103,31	66	80,29	77,05	61,4
3	105,56	66,11	79,45	85,57	70,41
4	101,39	64,31	75,59	80,72	63,9
5	100,35	64,37	75,3	79,48	61,51
6	100,64	64,56	78,93	79,53	69,39
7	101,94	64,05	73,78	80,29	57,2
8	101,8	68,56	78,95	76,49	60,27

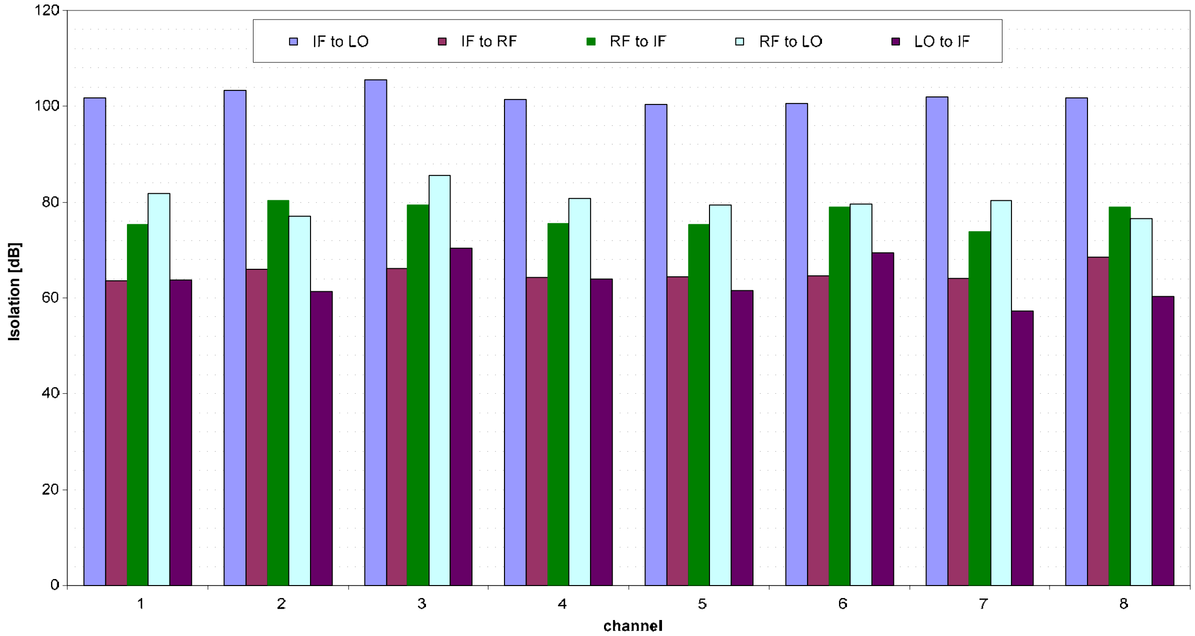

Figure 22. Isolation.

The isolation measurement's results are shown in Table 10 and Fig. 22. The most critical is the isolation behind the local oscillator and the output downconverter (intermediate frequency). The solution that has been assumed is sufficient for this application.

6. Mechanical Design

The board must fit in a 6-unit height Euro crate. (Dimensions: height = 233mm, width: 160 mm). The thickness of the board should be 1,2mm minimum and 1.6mm maximum. The front panel should be 4TE size (19,8mm x 261,3mm). The front panel connectors for the 8 RF inputs (RF_1.... RF_8 placed on the "top" of the board) and 8 *IF* outputs (IF_1....IF_8 placed below the RF input multi connector) are coaxial connectors, a proposed type is a FME008P102
The 8 pole coax connector is housed in a sub D size 5 (like 37pin). The type number form is FM8W8S-K121

The LO input connector should be a SMA type, e.g. SUHNER SMA type. This Input should be placed in the lower part of the front panel. The SMA connectors and sockets are preferred for different application, because they characterize a low reflection coefficient and good mechanical durability.

The LO Signal is splitted by a eight way - zero degree power splitter. Therefore a power splitter with ten outputs is necessary. As for now, only 8 way splitters are available, e.g. JEPS-12 –10 from Mini Circuits this splitter can be used. All unused output ports should be terminated with 50Ω.

The individual modules should be fitted with shielding to ensure appropriate immunity against unwanted interstage coupling, external noise sources and unwanted RF radiation.
Each of the eight mixer circuitries should have own metal-shielded housing, e.g. PFL2 (Farnel 522-120) For additional shielding the complete board should be housed in a cassette, e.g. Schroff.

The board should be the eight multilayer board:

Layer 1, 7 and 8 should be Power supply, intermediate frequency signal layers. There should be rubout layers for ground. Layer 2 and 4 should be ground. Layer 6 should be +5 Volt distribution. RF-Signals should be placed as CPW strip lines on layer 3 and 5.

Power Supply:

P1 Connector
+5Volts: Pins 32A, 32B, 32C (Dig. 5V)
GND (dig) Pins 9C,11A,15A,17A,19A.20B,23B

P2 Connector is a power supply connector 96 Pin abc rows in use.
+15 Volts Pins 1A,1B, 1C not used
GND Pins 2A,2B, 2C

-15 Volts Pins 3A,3B, 3C (generates ana-5V)
+5 Volts Pins 32A,32B,32C (Ana 5V)
-5 Volts Pins 30A,30B,30C not used
GND (dig) Pins 31A,31B,31C

-5 [*V*] should be generated from –15 [*V*] with a Voltage regulator +and -5 Volt analogue supply for the active Mixers and the IF Amplifiers should be separately filtered by 33mH Coils and 22µF and 220nF capacitors in parallel (one Filter for all eight channels).

7. Specification of The Downconverter

Parameters:	
RF Data	
Input frequency	1.3 GHz +/-10 MHz (-3 dB)
Nominal Input power range	-20 to +3 [dBm]
Input impedance	50[Ω]
Input VSWR	max. 1.5:1 desired, 1.8:1 acceptable
Input damage level	23 [dBm]
LO input requirements	
Input frequency	1.3 GHz +/- 100 [MHz] (-3[dB])
Input power	max. 0.5[W]
Input impedance	50 [Ω] nom
Input VSWR	1.5:1 desired, 1.8:1 acceptable
IF output requirements	
Output frequency	81 MHz +/-10 [MHz] (-3 [dB])
Output level	400mVpp @ RF in= -12 [dBm]
Output impedance	50[Ω]
Conversion parameter	
Isolation: RF and LO at IF	>60 [dBm]
Environmental condition	
Operating temperature range	-10 deg. C to +70 deg.C
Humidity	max 95 [%]

8. Conclusion

The revised board for the RF downconverter has been designed, manufactured and measured. The new idea of the digital RF feedback system gives better phase stability. Reconfiguration of the RF line will provide the test signal with better spectral purity. This design is the first step to a realization of very high linearity elements of RF feedback system in TTF2 project.

- Advantages

Change of intermediate frequency to higher (form 250kHz) makes it possible to shift signal's frequency out of range of electromagnetic noise spectrum in the surroundings of the accelerator. The increase of intermediate frequency makes it possible to decrease relative jitter of feedback signal (for IF_1=250kHz ~ $0,4 \cdot 10^{-3}$ %, for IF_2 =81MHz ~ $1,23 \cdot 10^{-6}$ %).

- high 1dB compression point: 7,5dBm(*Pin*), 13dBm(*Pout*) min. values for 1st channel,
- IIP3: 21, OIP3 26,5dBm of 8th – min. values for 8th channel
- good isolation:57dB *LO* to *IF* – min. value for 7th channel

- Disadvantages

Change of intermediate frequency for higher - 81MHz, increases the inter-channel crosstalk. The minimum value is: 50,84 dB between 1st and 7th channel.

To assure higher linearity and better inter-channel crosstalk new downconverters' PCB will be made (phenomena on via-hole and electromagnetic coupling will be considered, so that it will get required level of parameters). Advisable is precise electromagnetic analysis of printed circuit of downconverter. To improve the parameters, local feedback system for individual components and modules will be used.
In the downconverter system it would be worth to apply a VGA to use whole amplitude range of ADC, which will decrease the level of the quantization noise.

9. Development

In the future research, the main objective will be:

- to design the downconverter that has better stationary parameters and can give signal with lower intermodulation
- to adapt the downconverter to work in the accelerator environment.
- to improve the inter-channel crosstalk.

Additional element will be measuring of internal phase and amplitude noise of downconverter and optimization in perspective of requirements for RF Feedback System application.

Acknowledgement

I would like to thank Gounther Mooller and Henning Weddig for understanding and discussion, support. I would like to thank Dr. Stefan Simrock who gives me the opportunity to work in his group and supported me in all circumstances!

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References

[1] In cooperation, "Downconverter 2 - lp. 7548-00ML", *DES*Y, 2002
[2] S.A. Mass, "Microwave Mixer", Artech House, 1993
[3] J. Baranowski, G. Czajkowski, "Electronic Circuit, Vol. 2 - Nonlinear and impulse circuits" (in Polish) WNT, 1994
[4] D.M. Pozar, "Microwave Engeenering", John Wiley & Sons, Inc., 1998
[3] W.A. Davis, K. Agarwa, "Radio Frequency Circuit Design", John Wiley & Sons, Inc., 2001
[4] http://www.analog.com
[5] http://www.hittite.com

Appendix

Schematics diagrams of the downconverter board

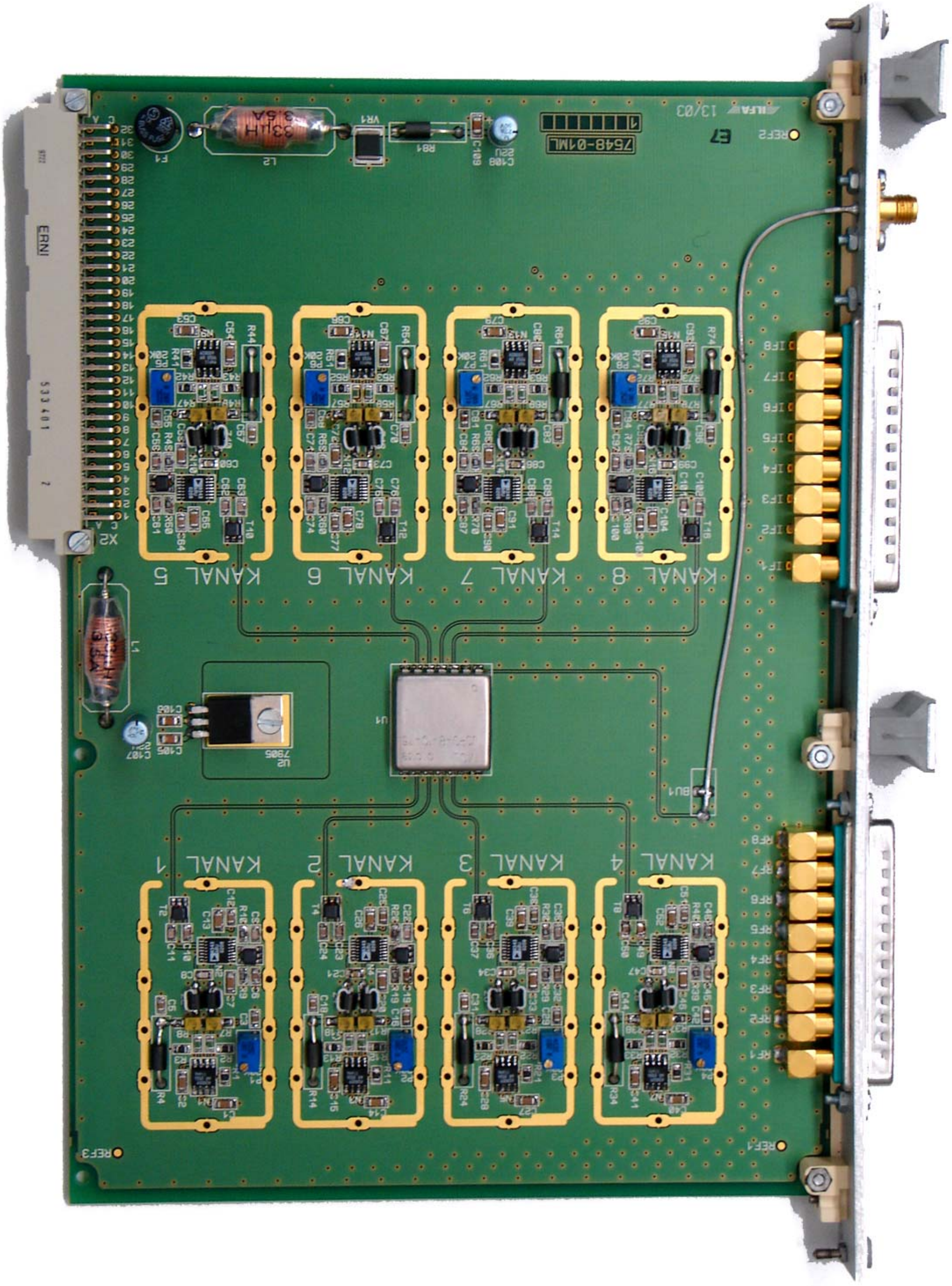
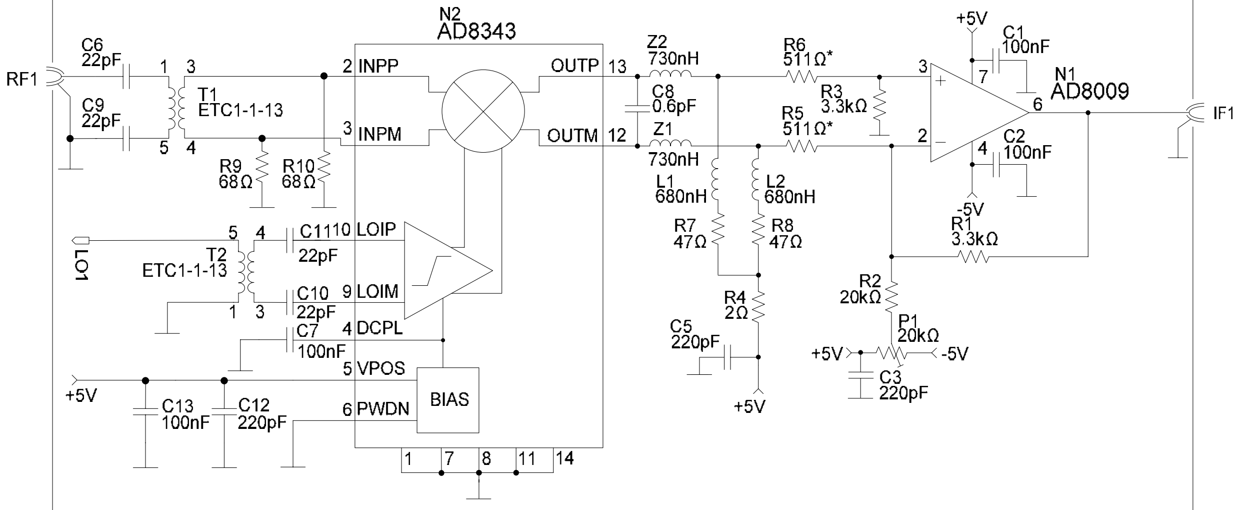


Figure 23. Picture of the downconverter board.



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Deutsche Elektronen-Synchrotron
Notkestraße 85, 22607 Hamburg

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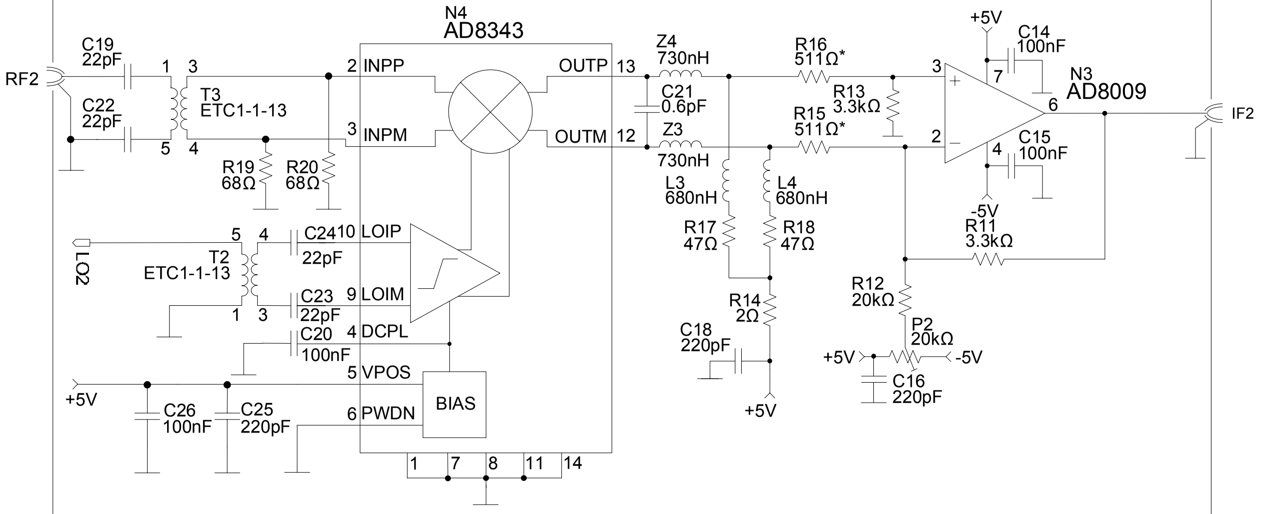
Design by:	Tomasz Filipek		
Date:	Friday, January 14, 2005		Sheet 1 of 9



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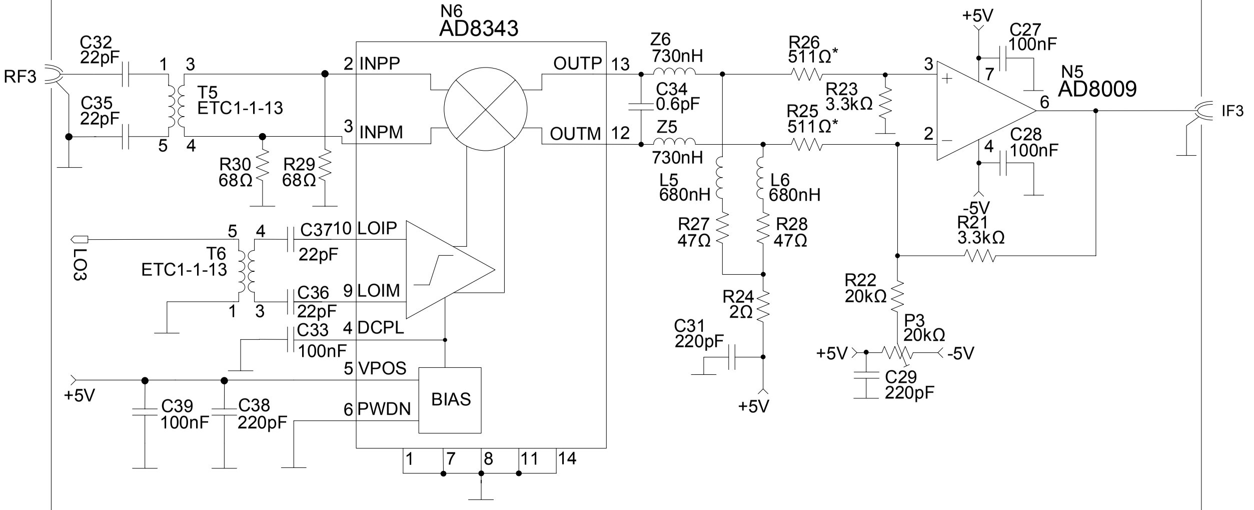

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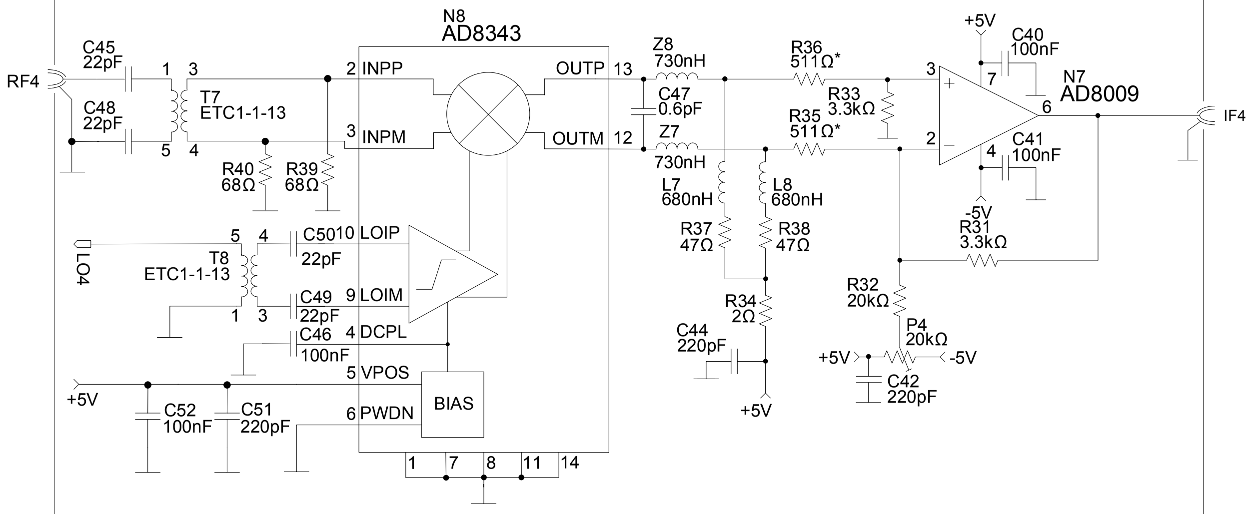

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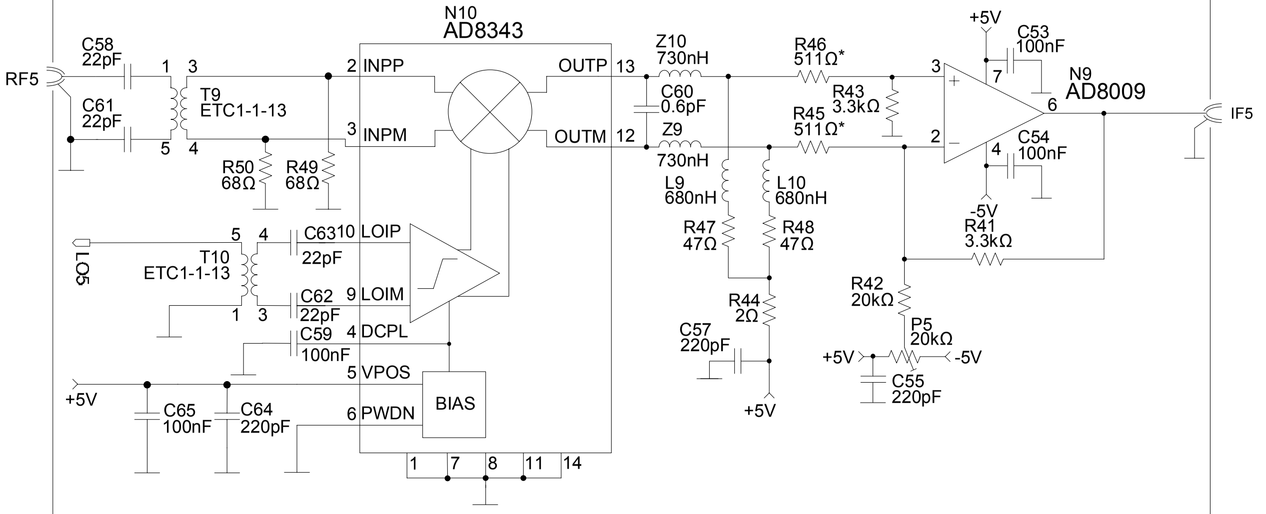

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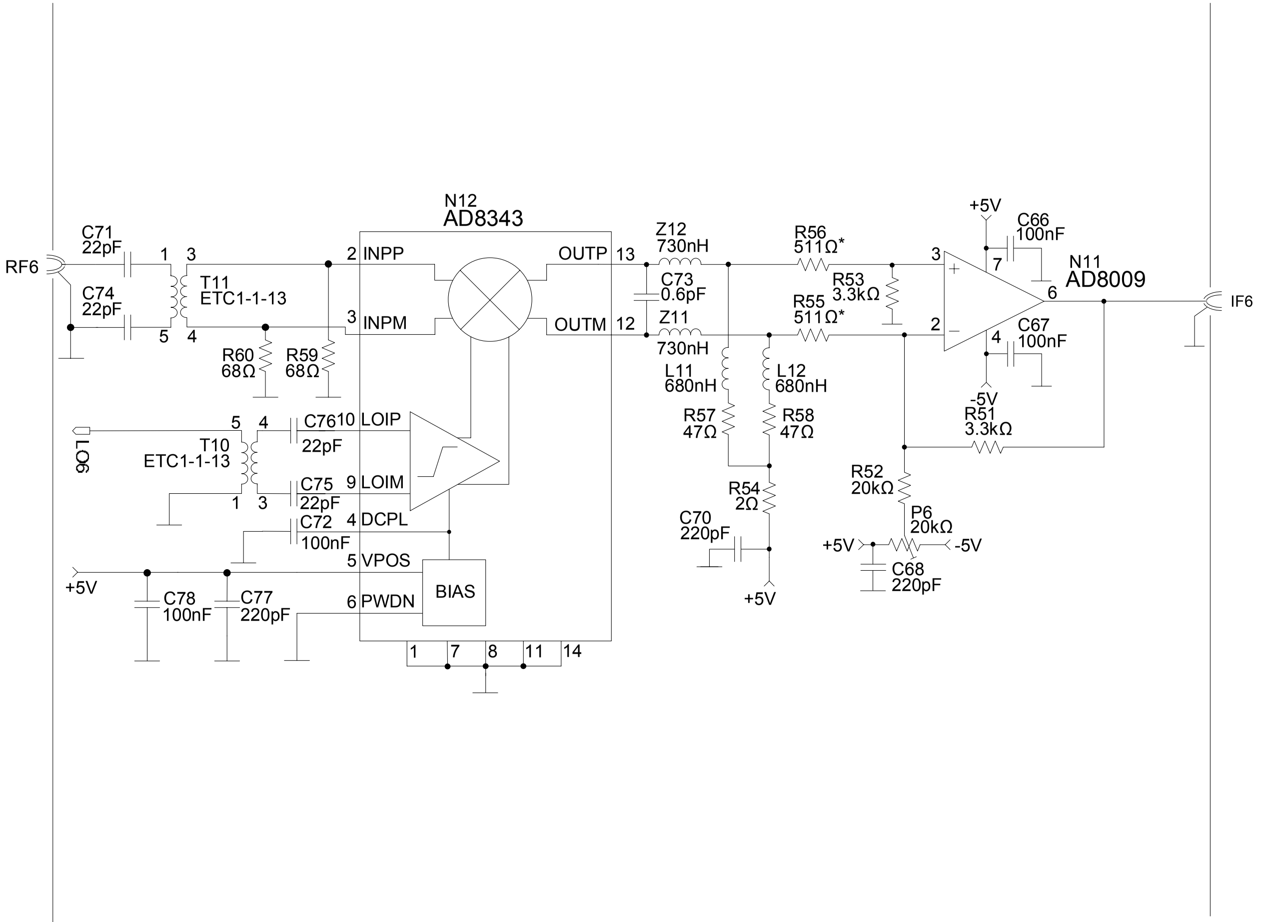
Downconverter

Channel 5

Sheet 5 of 9



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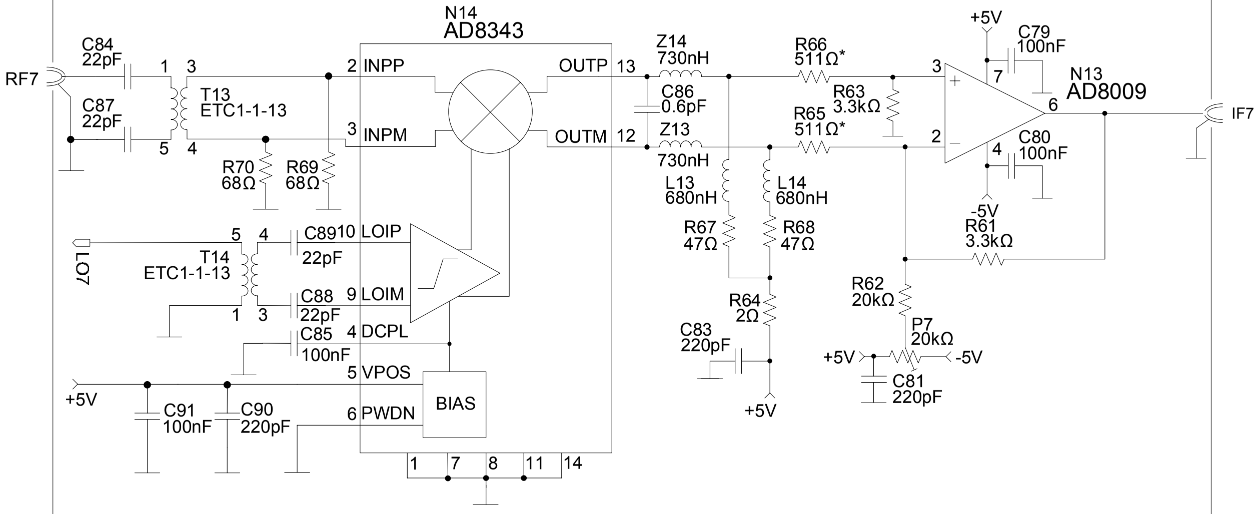
Project

Downconverter

Channel 6

Sheet 6 of 9



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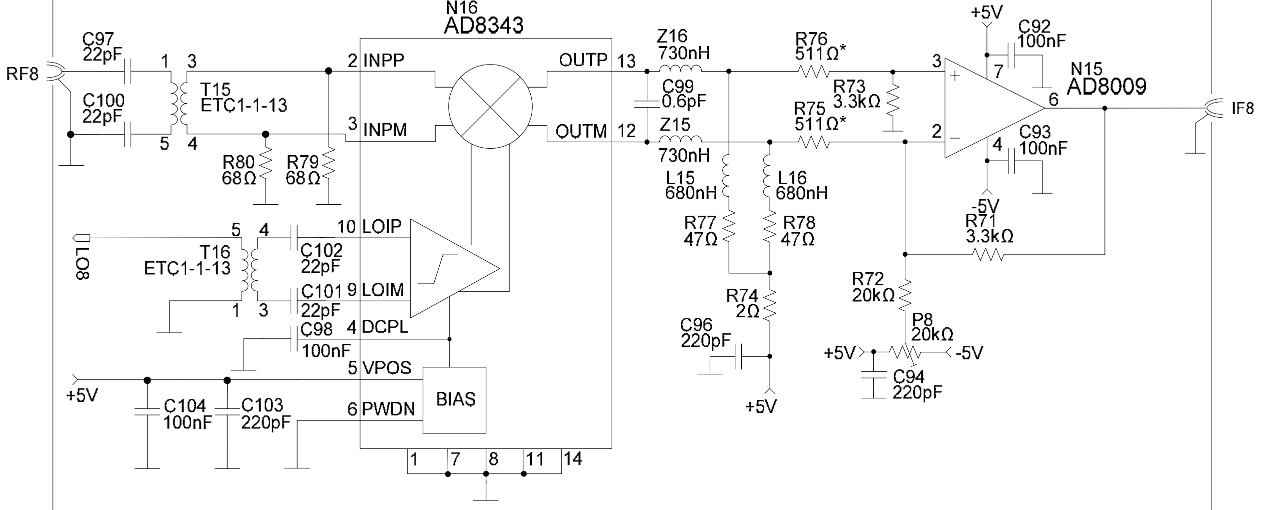
Project

Downconverter

Channel 7

Sheet 7 of 9



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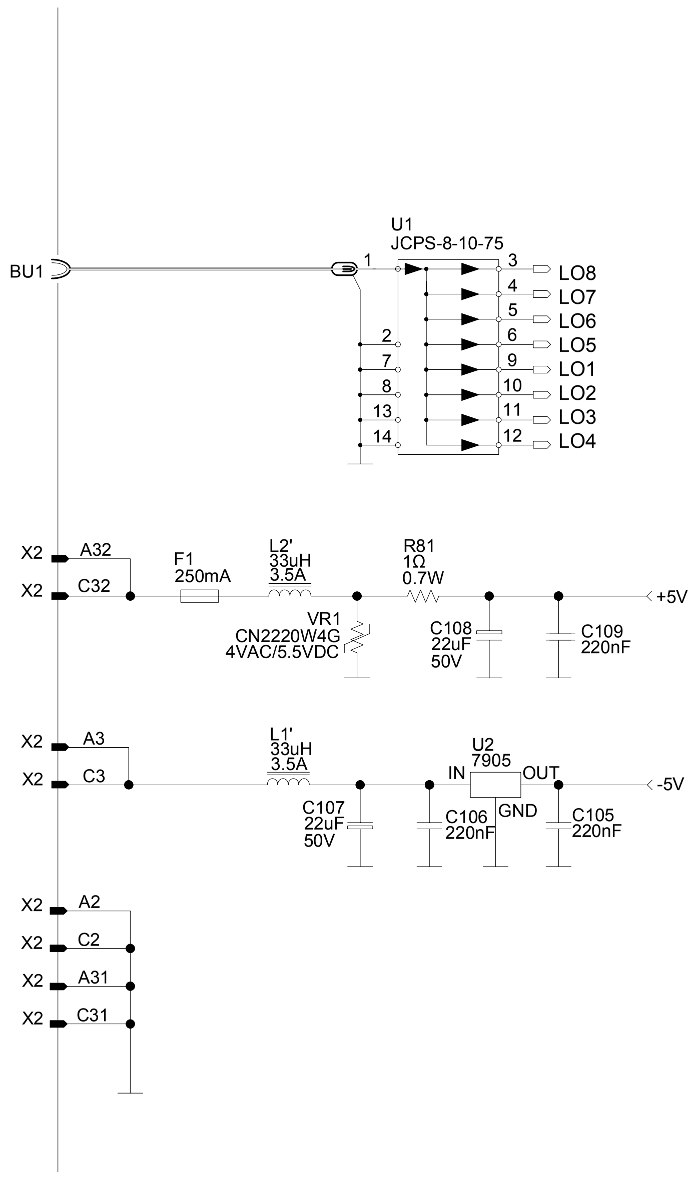

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Date: Friday, January 14, 2005

Project

Downconverter

Power Supply

Sheet 9 of 9