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Design and Simulation of FPGA Implementation of RF Control System for Tesla Test Facility

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ABSTRACT

This paper presents a new FPGA based solution of the Low Level RF Control System for the TESLA Test Facility. The LLRF Control System is responsible for maintaining the constant amplitude and phase of accelerating field in the cavities in the accelerator's cryomodules driven by single klystron (up to 32 cavities). To obtain shorter processing time and less complicated hardware an FPGA based solution was selected. The proposed simulation has been simulated in software, and appeared to be faster and less complex than DSP based solutions.

Keywords: TESLA, DESY, FPGA, DSP, datapath architecture, high energy physics

1. INTRODUCTION

The TESLA is a linear e^+ e^- collider, using superconducting accelerating structures. The electron and positon beams will be accelerated by standing wave resonators. To assure good focusing and monoenergetic beams, the constant amplitude and phase of the accelerating field is required. However the superconducting cavities are subjected to different factors influencing their geometry and resonance frequency - eg. microphoning, Lorentz force detuning and the others. Therefore a special "Low Level RF Control System" is required to keep the amplitude and phase of the accelerating field constant. The simple proportional regulator has been proposed, however it is possible to evaluate others, more sophisticated algorithms.

2. THE HARDWARE

The accelarating field in the cavity is a sinusoidal standing wave with frequency of 1.3 GHz. To assess the effective amplitude and phase of accelerating field, the field is sampled in each cavity, which results in 32 field values for each set of cryomodules controlled by the single LLRF Control System. The sampled voltage is proportional to the instantaneous field value, however sensitivity of probes may be different, and the connection cables may introduce additional phase shift - both of these effects need to be compensated when calculating the mean accelerating field value.

To allow further digital processing, the 1.3 GHz signals are down converted to 250 kHz, preserving the amplitude and phase information. These signals are sampled with A/D converters and input into the DSP block.

The output signals from the DSP block drive the Vector Modulator at the input of the power klystron - controlling directly the in-phase and quadrature components of accelerating field. The detailed description of the LLRF system may be found in[1] and.[2]

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3. ALGORITHM OF THE CONTROL SYSTEM

The intermediate frequency signal obtained after the down-conversion of original 1.3 GHz signal may be described as follows (where $\omega_0 = 2\pi f_0 = 2\pi 250$ kHz):

$$V_{IF}(t) = A(t)\cos(\omega_0 t + \varphi(t)) \tag{1}$$

which is equivalent to the form:

$$V_{IF}(t) = A(t)\,(\cos\omega_0 t\cos\varphi(t) - \sin\omega_0 t\sin\varphi(t)) \tag{2}$$

Instead of dealing with amplitude and phase of the V_{IF} signal we can introduce the analytical signal at frequency f_0

$$V(t) = A(t)\,(\cos\varphi(t) + i\sin\varphi(t))\cdot e^{i\omega_0 t} \tag{3}$$

with real (in-phase) component $I(t)$ and imaginary (quadrature) component $Q(t)$ defined as follows:

$$I(t) = A(t)\cos\varphi(t) \tag{4}$$
$$Q(t) = -A(t)\sin\varphi(t) \tag{5}$$

The intermediate frequency signal is sampled with frequency of 1 MHz, and each two consecutive samples may be used to assess the instantaneous values of $Q(t)$ and $I(t)$.

Let's assume, that the "zero" point on time axis has been selected so, that $\cos(\omega_0 t_0) = 1$. Then we can denote the samples taken around the t_0 as follows:

$$V_{IF,-1} = V_{IF}\left(t_0 - \frac{T}{4}\right) \tag{6}$$
$$V_{IF,0} = V_{IF}(t_0) \tag{7}$$
$$V_{IF,1} = V_{IF}\left(t_0 + \frac{T}{4}\right) \tag{8}$$
$$V_{IF,2} = V_{IF}\left(t_0 + \frac{T}{2}\right) \tag{9}$$
$$V_{IF,3} = V_{IF}\left(t_0 + \frac{3T}{4}\right) \tag{10}$$

then we get the following simple relationships:

$$V_{IF,-1} = V_{IF,3} = A(t)\sin\varphi(t) \tag{11}$$
$$V_{IF,0} = A(t)\cos\varphi(t) \tag{12}$$
$$V_{IF,1} = -A(t)\sin\varphi(t) \tag{13}$$
$$V_{IF,2} = -A(t)\cos\varphi(t) \tag{14}$$

However, in the real system, we have to assume, that our measurement channel introduces an additional phase shift φ_c (the c index denotes the number of cavity in a cryomodule), and the amplification error K_c , so in fact the measured signal is:

$$V_{IF}(t) = K_c A(t)\cos(\omega_0 t + \varphi_c + \varphi(t)) \tag{15}$$

and the above relationships have a different form:

$$V_{IF,-1} = V_{IF,3} = K_c A(t)\sin(\varphi_c + \varphi(t)) \tag{16}$$
$$V_{IF,0} = K_c A(t)\cos(\varphi_c + \varphi(t)) \tag{17}$$
$$V_{IF,1} = -K_c A(t)\sin(\varphi_c + \varphi(t)) \tag{18}$$
$$V_{IF,2} = -K_c A(t)\cos(\varphi_c + \varphi(t)) \tag{19}$$

$$V_{IF,0} = K_c A(t)\ (\cos\varphi(t)\ \cos\varphi_c - \sin\varphi(t)\ \sin\varphi_c) \tag{20}$$
$$V_{IF,1} = -K_c A(t)\ (\cos\varphi(t)\ \sin\varphi_c + \sin\varphi(t)\ \cos\varphi_c) \tag{21}$$
$$V_{IF,2} = -K_c A(t)\ (\cos\varphi(t)\ \cos\varphi_c - \sin\varphi(t)\ \sin\varphi_c) \tag{22}$$
$$V_{IF,-1} = V_{IF,3} = K_c A(t)\ (\cos\varphi(t)\ \sin\varphi_c + \sin\varphi(t)\ \cos\varphi_c) \tag{23}$$

If we assume, that the $\varphi(t)$ and $A(t)$ signals are varying slowly and we can consider them to be constant during the single period of V_{IF}, then we can replace the $I(t)$ and $Q(t)$ signals with the I and Q, which are also constant during the single V_{IF} period.

Basing on the above assumption and substituting equations 4 and 5 into the 20 - 23, we get

$$V_{IF,0} = K_c Q\cos\varphi_c + K_c I\sin\varphi_c \tag{24}$$
$$V_{IF,1} = -K_c Q\sin\varphi_c + K_c I\cos\varphi_c \tag{25}$$
$$V_{IF,2} = -K_c Q\cos\varphi_c - K_c I\sin\varphi_c \tag{26}$$
$$V_{IF,-1} = V_{IF,3} = K_c Q\sin\varphi_c - K_c I\cos\varphi_c \tag{27}$$

From the above equations we can find the formulas for calculating I and Q for each quarter k of period from two consecutive samples: $V_{IF,k-1}$ and $V_{IF,k}$:

$$k=0 \quad I_c = -\frac{\cos\varphi_c}{K_c}V_{IF,k-1} + \frac{\sin\varphi_c}{K_c}V_{IF,k} \tag{28}$$
$$Q_c = \frac{\sin\varphi_c}{K_c}V_{IF,k-1} + \frac{\cos\varphi_c}{K_c}V_{IF,k} \tag{29}$$
$$k=1 \quad I_c = \frac{\sin\varphi_c}{K_c}V_{IF,k-1} + \frac{\cos\varphi_c}{K_c}V_{IF,k} \tag{30}$$
$$Q_c = \frac{\cos\varphi_c}{V}_{IF,k-1} - \frac{\sin\varphi_c}{K_c}V_{IF,k} \tag{31}$$
$$k=2 \quad I_c = \frac{\cos\varphi_c}{K_c}V_{IF,k-1} - \frac{\sin\varphi_c}{K_c}V_{IF,k} \tag{32}$$
$$Q_c = -\frac{\sin\varphi_c}{K_c}V_{IF,k-1} - \frac{\cos\varphi_c}{K_c}V_{IF,k} \tag{33}$$
$$k=3 \quad I_c = -\frac{\sin\varphi_c}{K_c}V_{IF,k-1} - \frac{\cos\varphi_c}{K_c}V_{IF,k} \tag{34}$$
$$Q_c = -\frac{\cos\varphi_c}{K_c}V_{IF,k-1} + \frac{\sin\varphi_c}{K_c}V_{IF,k} \tag{35}$$

The above coefficients are calculated for each cavity during the calibration, and then stored into the RAM.

The mean accelerating field vector in the whole set of cryomodules is equal to:

$$I = \sum_{c=1}^{8} I_c \tag{36}$$
$$Q = \sum_{c=1}^{8} Q_c \tag{37}$$

To decrease the noise level, the estimated I and Q values are averaged with a simple single-pole low-pass IIR filter:

$$I_{av,k} = I_{av,k-1} + \alpha(I_k - I_{av,k-1}) \tag{38}$$
$$Q_{av,k} = Q_{av,k-1} + \alpha(Q_k - Q_{av,k-1}) \tag{39}$$

And finally the averaged I and Q estimates are compared with the desired values I_{set} and Q_{set} to calculate the control values.

$$I_{ctrl,k} = K_{fb,I}\,(I_{set,k} - I_{av,k}) \tag{40}$$
$$Q_{ctrl,k} = K_{fb,Q}\,(Q_{set,k} - Q_{av,k}) \tag{41}$$

The $K_{fb,I}$ and $K_{fb,Q}$ coefficients are the amplifications in feedback loop for real and imaginary components of the field vector.

However to compensate the predictable deterministic disturbances an additional "feed forward" compensation may be added, and finally the control system is described with the following equations:

$$I_{ctrl,k} = I_{ff,k} + K_{fb,I}\,(I_{set,k} - I_{av,k}) \tag{42}$$
$$Q_{ctrl,k} = Q_{ff,k} + K_{fb,Q}\,(Q_{set,k} - Q_{av,k}) \tag{43}$$

4. IMPLEMENTATION

The FPGA design was performed using the Xilinx System Generator tools. Such solution shortened the design and testing time, allowing for integration of simulated FPGA project with Matlab model of the cavity.[3]

Some of the block diagrams presented in the article are just slightly processed original design diagrams, however due to legibility, other blocks are shown only as simplified drawings.

When designing the FPGA implementation the hardware consideration were to be taken into account. The parallel connection of 32 A/D converters to the FPGA circuit could be too difficult because of big amount of pins and lines used for ADC interfacing.

The required throughput (1 Msample/sec upgradeable to 10 Msamples/sec) allows for multiplexing of ADCs. Finally the solution with 4 ADC input blocks (called ADC Conditioners), each supporting 8 ADCs connected to common bus, has been selected. However both the number of ADC Conditioners, and the number of ADCs serviced by the single Conditioner can be easily changed.

The general structure of the Control System is shown in the figure 1.

The whole DSP system has pipelined datapath architecture which allows parallel processing of data on different stages of the system. The processed data are accompanied on each stage with the cavity and quarter numbers, or with "data ready" signal to allow the proper synchronization of the whole system.

The first block in the datapath is the ADC Conditioner.

4.1. ADC Conditioner

The structure of ADC Conditioner block is shown in the figure 2

After the ADC conversion is finished, in each clock cycle a data from the next ADC is transferred. Therefore a FIFO queue is necessary to separate the $V_{IF,k-1}$ and $V_{IF,k}$ samples for the same cavity from the data stream. The "Process data" signal enables the FIFO queue only when new data are provided, because the sampling period will be longer then 8 system clocks.

The $V_{IF,k-1}$ and $V_{IF,k}$ samples are then processed according to equations 28 to 35. Because the coefficients used in the calculation depend on both ADC number (cavity number) and the quarter number, both these numbers are used to address the RAM memory, which stores the appropriate $\pm\frac{\cos\varphi_c}{K_c}$ and $\pm\frac{\sin\varphi_c}{K_c}$ values. The ADC signal conditioning - consisting of complex $[I,Q]$ vector scaling and rotation is performed by "Matrix Rotation" block, shown in the figure 3. On the output of Matrix Rotation blocks the complex estimates of accelerating field in particular cavity cell (Q_c and I_c) are available and are summed in the accumulator. The accumulator is preset in each sampling cycle with the Q_0 and I_0 values, and after 8 clock cycles it contains the total accelerating field in 8 cells of the cavity. The results from four ADC Conditioners are then added to get the estimate of mean accelerating field in the whole cryomodule (module "Vector Sum" in the figure 1).

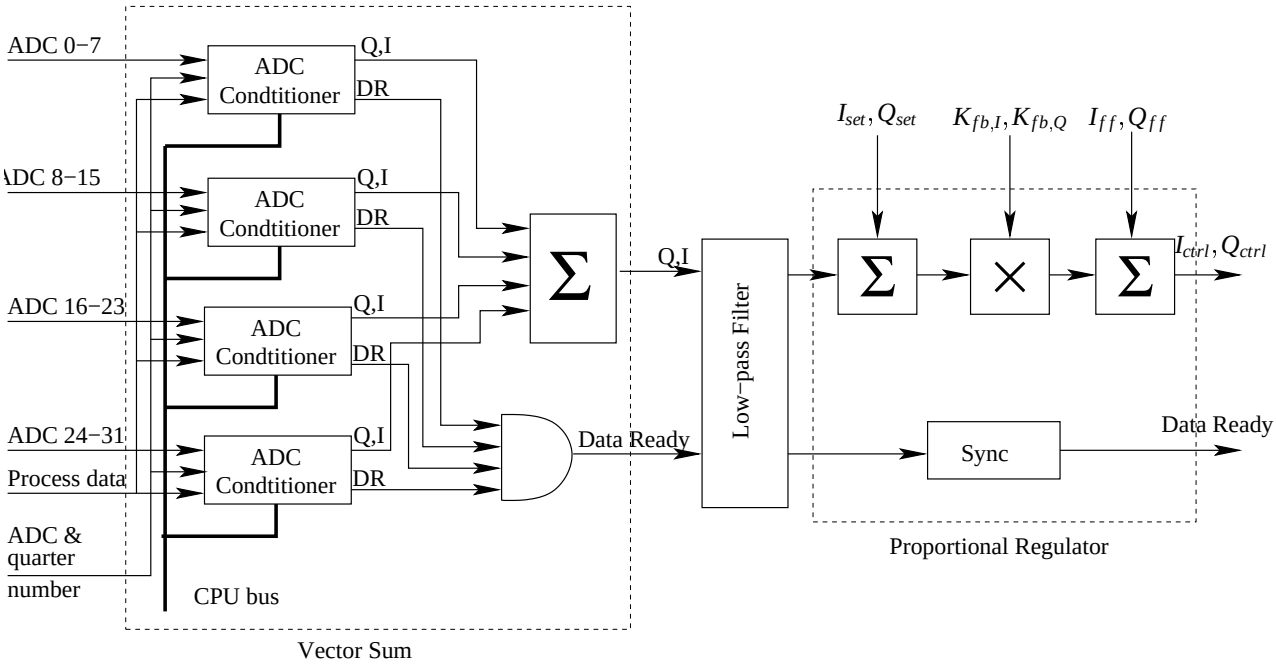

Figure 1. The general structure of the LLRF Controller System.

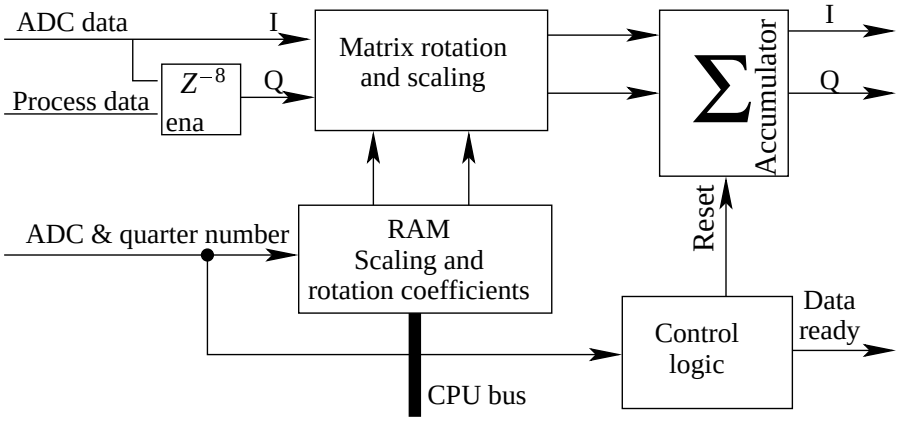

Figure 2. ADC conditioner system

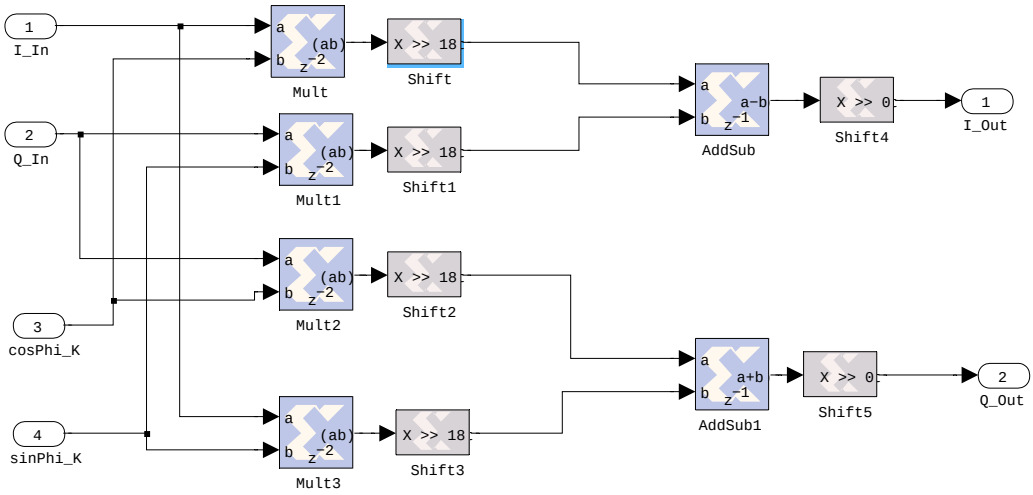

Figure 3. “Matrix Rotation” block.

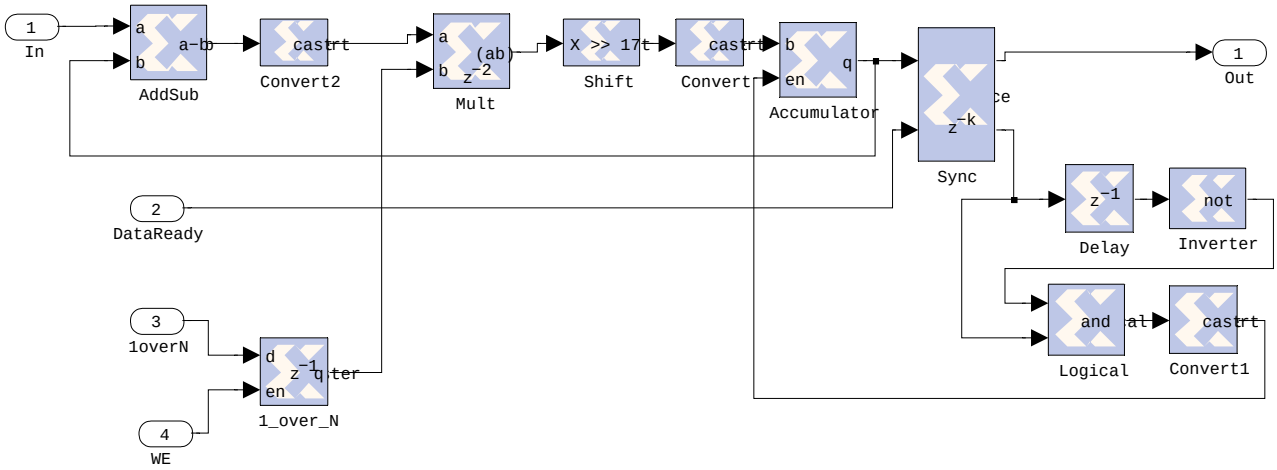

Figure 4. Low-pass filter

4.2. Low pass filter

The next block performs the low-pas filtering of accelerating field estimates, according to equations 38 and 39. The architecture of low-pass filter is shown in the figure 4

4.3. Proportional regulator with feedforward input

The last block calculates the Vector Modulator control voltages, according to the formulas 42 and 43.

Its structure is shown as the last section in the figure 1.

4.4. Performance of the implementation

The whole design was compiled into the Xilinx XC2V3000 FPGA. It took 20% of embedded multipliers, 3% of LUT’s, 3% of flip-flops, 12% of I/O blocks and 8% of RAM. The maximum clock frequency was equal to 103,85 MHz. The total signal processing latency was equal to 19 clock periods (190 ns at f_{clk} =100 MHz and 292 ns at f_{clk} =65 MHz).

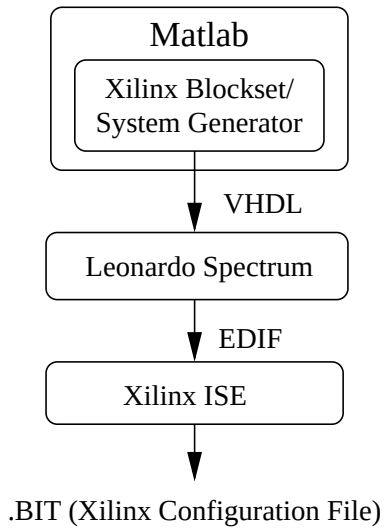

Figure 5. Design flow of the RF Control System.

5. REMARKS ON TOOLS

In the project the following GUI based design tools have been used:

- Matlab Version 6.1.0.450 Release 12.1
- Simulink Block Library 4.1
- Simulink blocks for use with the Control System Toolbox
- Xilinx System Generator v2.2
- Leonardo Spectrum 2002d.22
- Xilinx ISE 4.2.03i

The implementation and testing have been performed using the Matlab with Simulink suplemented with Simulink blocks for use with Control System Toolbox and Xilinx System Generator (ver. 2.2).

The VHDL code generated with Xilinx System Generator were compiled into the Xilinx bitstream by Leonardo Spectrum

The whole design flow is shown in the figure 5.

The Matlab based environment used for development of DSP IP core proved to be a really efficient tool, allowing for fast development and testing of DSP algorithm and then for easy implementing in the FPGA.

The DSP implementation used fixed point arithmetic and word length changes, as well as saturation mode could be implemented in a very easy way. Additionally the ability to switch between floating and fixed point calculations in the System Generator blocks allows to determine the rounding or quantization effects, helping to find the best word length for fixed point arithmetic.

The design environment also provided the very convenient tool (sync block) to solve the data sychronization problems typical for datapath architecture.

However a few problems occured, associated probably with still unfixed bugs on unimplemented features in these relatively new tools. Although it was possible to build libraries of reusable components, the system had problems with maintaining links to the library elements, especially when the implementation of particular element was changed. It was

really difficult to control propagation of changes introduced by editing of library contents or embedded library components, and sometimes different versions of the same library element were simultaneously present in the design, which lead to very frustrating errors.

6. CONCLUSIONS

The proposed solution offers much better speed comparing to the DSP based one. The FPGA based solutions allows us to assure the really fast processing especially for datapath architecture algorithms.

Additionally the “single chip” solution decreases the number of connections which should improve the reliability.

Using of programmable chip assures very high flexibility, even though it may be difficult to implement complex algorithms (which are rather better suited for DSP implementations).

Additionally the same hardware may be used for both system testing or calibration and for standard work of the system (depending on the configuration of the FPGA), which decreases the total cost of the implementation.

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